Company Profile

Founded on February 21, 1987 and headquartered in Hsinchu, Taiwan, TSMC pioneered the foundry business model by focusing solely on manufacturing customers’ semiconductor designs. As a pure-play semiconductor foundry, the Company does not design, manufacture, or market semiconductor products under its own brand name, ensuring that TSMC does not compete directly with its customers. Today, TSMC is the world’s largest pure-play semiconductor foundry, manufacturing more than 8,600 different products using 202 different technologies for over 440 different customers in 2013.

With a diverse global customer base, TSMC-manufactured semiconductors are used in a wide variety of applications covering various segments of the computer, communications, consumer, industrial and standard semiconductor markets.

Annual capacity of the manufacturing facilities managed by TSMC and its subsidiaries totaled 16.4 million 8-inch equivalent wafers in 2013. TSMC’s managed manufacturing facilities include three 12-inch wafer GIGAFAB™, four 8-inch wafer fabs, and one 6-inch wafer fab in Taiwan, as well as two 8-inch fabs at wholly owned subsidiaries: WaferTech in the United States and TSMC China Company Limited.

TSMC provides customer service through its account management and engineering services offices in North America, Europe, Japan, China, South Korea, and India. The Company employed more than 40,000 people worldwide at the end of 2013.
TSMC continued to lead the foundry segment of the semiconductor industry in both advanced and specialty process technologies. By leveraging the experience of 65nm and 40nm, TSMC successfully reached mass production of 28nm with excellent yield performance in 2013 featuring 28HP and 28HPM for high performance and 28LP and 28HPL for low power. Furthermore, TSMC delivered 20nm SoC and 16nm FinFET technology nodes on-schedule and successfully received initial customer tape-outs of 20nm technology. In addition to general-purpose logic process technology, TSMC supports the wide-ranging needs of its customers with embedded non-volatile memory, embedded DRAM, Mixed Signal/RF, high voltage, CMOS image sensor, MEMS, silicon germanium technologies and automotive service packages. TSMC’s subsidiaries TSMC Solid State Lighting Ltd. and TSMC Solar Ltd. also engage in researching, developing, designing, manufacturing and selling solid state lighting devices and related products and systems, and solar-related technologies and products, respectively.

The Company is listed on the Taiwan Stock Exchange (TWSE) under ticker number 2330, and its American Depositary Shares trade on the New York Stock Exchange (NYSE) under the symbol “TSM”.

2.1 Market/Business Summary

2.1.1 TSMC Achievements

In 2013, TSMC maintained its leading position in the total foundry segment of the global semiconductor industry, with an estimated market segment share of 49%. TSMC achieved this result amid intense competition from both established players and relatively new entrants to the business. Leadership in advanced process technologies is a key factor in TSMC’s strong market position. In 2013, 50% of TSMC’s wafer revenue came from manufacturing processes with geometries of 40/45nm and below.

2.1.2 Market Overview

TSMC estimates that the worldwide semiconductor market in 2013 reached US$322 billion in revenue, a 5% growth compared to 2012. Total foundry, a manufacturing sub-segment of the semiconductor industry, generated total revenues of US$37 billion in 2013, or 11% YoY growth.

2.1.3 Industry Outlook, Opportunities and Threats

Industry Demand and Supply Outlook

Following 16% growth in 2012, foundry segment growth again accelerated by double digits, to 11% in 2013, mainly driven by fabless market share gains over IDM and process technology advancement. TSMC forecasts total semiconductor market to grow 5% YoY in 2014. Over the longer term, due to: increasing semiconductor content in electronics devices, continuing market share gain of fabless, and increasing in-house Application-Specific Integrated Circuits (ASIC) from system companies, foundry sales are expected to display much stronger growth than the projected 4% compound annual growth rate (CAGR) for the total semiconductor industry from 2013 through 2018.

As an upstream supplier in the semiconductor supply chain, the condition of the foundry segment is tightly correlated with the market health of the 3Cs: communications, computer and consumer.

● Communications

The communications sector, particularly the handset segment, posted a modest 4% growth in unit shipments for 2013. Smartphones, which have much stronger growth and higher semiconductor content, have been leading the growth of the sector.

The continuing transition to 4G/LTE and LTE-Advanced handsets will bring positive momentum to the market. Smartphones with increasing performance, lower power and more intelligent features will continue to propel the buying interest of new handsets in 2014. The growing popularity of mid- to low-end smartphones in the emerging countries is also a new catalyst driving the growth of the sector.

Low power IC is an essential requirement among handset manufacturers. The SoC design for more optimized cost, power and form-factor (i.e. device footprint), plus the appetite for higher performance to run complicated software, will continue to accelerate the migration to advanced process technologies in which TSMC is already the leader.
2.2 Innovation Management

Innovation is the wellspring of TSMC’s growth, and is a part of all aspects of our business, from strategic planning, marketing and management, to technology and manufacturing. At TSMC, innovation means more than new ideas, it means putting ideas into practice.

2.2.1 Innovation at TSMC

In 2013 TSMC continued to invest in R&D with total R&D expenditure amounting to 8% of revenue, a level that equals or exceeds the R&D investment of many other high technology leaders. Along with the increase in budget, R&D staffing increased by 11%. TSMC has built an innovative working atmosphere to encourage employees to make their innovation ideas come true. The awards from around the world that TSMC has received demonstrate the outstanding performance of our talents.

2.2.2 Technology Leadership

TSMC recognizes that the technology challenge required to extend Moore’s Law, the business law behind CMOS scaling, is becoming increasingly complex. The efforts of the R&D organization are focused on enabling the Company to continuously offer its customers first-to-market, leading edge technologies and design solutions that contribute to their product success in today’s complex and challenging market environment. In 2013 the R&D organization met these challenges by introducing into manufacture an industry-leading 20nm technology. The 16nm technology, which is TSMC’s first integrated technology platform to make use of 3D FinFET transistors, has also met its development goals and is now in risk production. The R&D organization continues to strengthen the pipeline of technology innovations that are required to maintain technology leadership. Advanced
development of 10nm technology was completed, and entered full development, while 7nm technology is in the early development stage.

In addition to CMOS logic, TSMC conducts research and development on a wide range of other semiconductor technologies that provide the functionality our customers require for mobile SoC and other applications. Highlights achieved in 2013 include: production ramp of the CoWoStm (Chip on Wafer on Substrate) 3D packaging technology; extension of the 28nm technology for RF and embedded flash technologies; the first industry introduction of the BCD power technology into a 12-inch fab environment and, manufacturing readiness of TSMC’s first wide band gap Gallium Nitride (GaN) semiconductor technology for high frequency power applications.

TSMC maintains a network of important external R&D partnerships and alliances with world-class research institutions such as IMEC, the respected European R&D consortium, where TSMC is a core partner. TSMC also provides funding for nanotechnology research at leading universities worldwide to promote innovation and the advancement of nanoelectronic technology. In 2013, TSMC announced the formation of collaborative research centers with National Taiwan University and National Chiao-Tung University in Taiwan, and anticipates announcing the establishment of additional research centers in Taiwan in 2014.

Advance Technology Innovations
As the semiconductor foundry leader, TSMC continued to provide technology innovations to lead the foundry segment of the semiconductor industry in both advanced and “More-than-Moore” process technologies. Not only was it the first foundry to provide 65nm and 40nm production capacity, TSMC also became the first foundry to offer volume production of 28nm, with our first-to-market 28nm high-k/metal gate (HKMG) technology portfolio. Furthermore, TSMC delivered the world’s first 28nm High-k/Metal Gate triple gate oxide technology (28HPT) in 2013.

- **28nm Technology**
  TSMC delivered the world’s first 28nm High-k/Metal Gate triple gate oxide technology (28HPT). This technology provides 10% faster speed compared to the 28HPE technology while keeping the same leakage power. 28HPT is qualified for production in both Fab 12 and Fab 15 with equivalent yield to 28HPE.

- **20nm Technology**
  TSMC’s 20nm technology was successfully qualified for volume manufacture.

- **16nm Technology**
  The 16nm technology features FinFET transistors with a third generation High-k/Metal Gate process, a fifth generation of transistor strain process, and advanced 193nm lithography. FinFET transistors offer substantial power reduction at the same chip performance compared to transistors built with the traditional planar structure, which is essential for advanced mobile applications. In 2013, the R&D organization successfully verified the process development test vehicle (TV1R), provided customers with version 1.0 design kits (design rules and SPICE models) and offered two public cyber shuttles.

More than 10 customers and IP vendors took the shuttles and verified their IP. The 16nm technology has completed manufacturing qualification with good yield.

Awards Over the Years
- 7 IEEE Fellows (Incl. 1 life fellow)
- 1 U.S. National Academy of Engineering Member
- 1 IEEE Medal of Honor
- 1 IEEE Andrew S. Grove Award
- 1 IEEE Cledo Brunetti Award
- 1 IEEE Robert N. Noyce Medal
- 1 IEEE Corporate Innovation Award
- 1 “Stars of Asia” from Business Week
- 1 Robert N. Noyce Award from the SIA
- 1 Akira Inoue Award from SEMI
- 1 Nikkei Asia Prize for Regional Growth
- 1 Outstanding Scientific and Technological Worker Award from the Executive Yuan of the Republic of China
- 1 First-ever Outstanding Nano-Tech Award from the Ministry of Economic Affairs of the Republic of China
- 16 National Industrial/Enterprise Innovations Awards, the Taiwan government’s most prestigious award for innovation achievement.
10nm Technology
In 2013, saw the introduction of 10nm technology into development. This 10nm technology will offer substantial power reduction for the same chip performance compared to earlier technology generations. Development activities in 2014 will focus on manufacturing baseline process setup, yield learning, transistor performance improvement, and reliability evaluation. TSMC will enter 10nm risk production in 2015 and mass production in 2016.

Lithography
2013 was a productive year in 16nm lithography development with the technology reaching the risk production stage. Several novel patterning techniques were developed for 48nm pitch Fin patterning. These techniques overcame the challenge of high aspect ratio topography of 3D device structures. Besides patterning challenges, defect reduction on the high aspect ratio topography also required special engineering efforts. Several key solutions were developed in 2013, such as improvement in tool and process recipe co-optimization, and enhanced defect-monitoring methodology. The development of optimum automation and Advanced Process Control systems, including enhanced tool control and stability, resulted in significant reduction of rework rate and cycle time, helping to drive faster learning in both defect reduction and yield improvement.

Several new techniques were introduced during 2013 to enable the successful launch of 10nm development. While the immersion lithography process will be extended to the 10nm node, the double patterning technique that was developed for the 20nm and 16nm nodes is insufficient to meet 10nm requirements. Multiple patterning becomes essential to enable high yield manufacturing. To further stretch the patterning capability of optical lithography, significant learning in material processing, image modeling, and defect control has been achieved to make the 10nm process viable.

In 2013, TSMC took delivery of a NXE3300 extreme ultraviolet (EUV) scanner, and exposed its first wafers after successful installation. While we see a clear advantage in process simplification by the use of EUV as opposed to multiple patterning with optical immersion lithography, insufficient power of the EUV light source is our major concern.

Multiple e-beam direct-write lithography (MEB DW) not only has the potential for economical imaging critical layers, but it also may offer cost reduction potential for non-critical layers and 450mm wafers. It is being developed to meet the need of 7nm node imaging and beyond. A TSMC team from the design, CMOS, MEMS, and packaging areas is jointly developing and fabricating the digital pattern generation (DPG) module for the Reflective E-Beam Lithography (REBL) system of KLA-Tencor. The first DPG test chip, which was a collaborative effort between TSMC and KLA-Tencor, was tape out in the third quarter of 2013.

Mask Technology
Mask technology is an integral part of our advanced lithography. In 2013, we completed the development of mask technology for the 16nm node and made solid...
progress on development for the 10nm node. In the meantime, continued progress is being made on the mask technology for EUV lithography. Working with suppliers, we continue to drive down counts of native defects on mask blanks. In addition TSMC continues to work with several industrial consortia in developing the infrastructure of EUV mask technology.

Integrated Interconnect and Packaging

- **3D IC**
  TSMC achieved a new industry landmark in 2013 with the ramp up to volume production of a new turnkey system integration solution called CoWoS™ (Chip on Wafer on Substrate). The CoWoS™ solution is integrated with TSMC’s advanced silicon technologies to provide customers with alternatives for system level integration compared to the traditional SoC approach. The technology has passed customer product qualifications with 28nm FPGA products. At 20nm, development continues and we expect customer tape-outs in the first half of 2014. We successfully demonstrated 3D IC stacking of an application processor and wide I/O DRAM in 28HPM technology through transistor stacking (TTS) TSV technology, and completed 16nm TSV process development.

- **Advanced Package Development**
  TSMC offers a wide variety of lead-free flip chip packaging technologies. In 2013 TSMC qualified for manufacture at 20nm an innovative Bump-on-Trace (BoT) packaging technology with an ultra-fine pitch (80µm) copper (Cu) bump that is suitable for mobile/handheld devices. Additionally, lead-free flip chip packaging was enhanced for ultra large die size (≥600 mm²) for high performance applications (GPU/CPUs/FPGA/Networking Processor).

- **Advanced Interconnect**
  Development of low resistance Cu and low capacitance dielectric continued to be the primary focus in 2013. At the 16nm node, a novel dielectric scheme has been developed that reduces the capacitance between copper lines. For the 10nm node and beyond, we have developed a new spacer-patterning scheme that allows copper line spacing to be reduced and minimizes signal delay. The effective resistivity of copper lines developed with these advanced processes is highly competitive and is lower than that projected by the International Technology Roadmap for Semiconductors (ITRS).

Advanced Transistor Research

The increased performance and lower power requirements of advanced logic technologies require constant innovation in transistor architecture and materials. TSMC is at the forefront of research in these areas, with particular focus on non-silicon channel materials such as germanium and III-V compounds because of their desirable performance and power characteristics. As an example of the progress being made in this area, our research team recently announced at the 2013 International Electron Devices Meeting world record-breaking transistor performance for both Germanium (Ge) channel PMOS FinFET and Indium Arsenide (InAs)
Specialty Technology
TSMC offers a broad mix of technologies to address the wide range of applications that customers are engaged in. The Company enhanced its SoC roadmap to address the needs of specialty applications in the mixed-signal, RF markets, high voltage power management ICs, high voltage IC’s for display, MEMS, and embedded memory.

- **Mixed Signal/Radio Frequency (MS/RF) Technology**
  TSMC has successfully verified customer products in 28nm technology for RF CMOS applications (28LP-RF) that are aimed at next generation RF transceivers (e.g. 4G LTE). Higher performance analog and RF solutions are also in development at the 20nm node. TSMC developed and transferred to manufacturing a first generation 0.18µm complementary buried channel MOS (CBCMOS) technology.

- **Power IC/BCD Technology**
  TSMC released 0.13BCD technology, the first BCD technology to be implemented in a 12-inch fab. The R&D team also completed development and qualified for manufacture the wide band gap material GaN in a high electron mobility transistor (HEMT) configuration for high power, high frequency applications. The 55HV technology was qualified targeting high quality mobile displays, while C015HV was released targeted at the large panel market. TSMC achieved several important milestones in embedded flash technologies. At the more mature 65nm/55nm node, NOR based cell technologies including 1-T cell and Split-Gate cell successfully completed customer qualification. At the 40nm node, the split-gate cell technology has been shipped for both automotive and consumer applications. Embedded flash development for the 28LP and 28HPM platforms is underway for low leakage applications such as smartcard, MCU and Automobile.

2.2.3 **Open Innovation Platform® (OIP)**
Innovation has long been both an exciting and challenging proposition. Competition among semiconductor companies is becoming more active and intense in the face of increasing customer consolidation, and the commoditization of volume and speeding time-to-market and, ultimately, time-to-revenue. It features:

- The foundry segment’s earliest and most comprehensive EDA certification program delivering timely design tool enhancement required by new process technologies; and
- The foundry segment’s largest, most comprehensive and robust silicon-proven intellectual properties (IPs) and library portfolio; and
- Comprehensive design ecosystem alliance programs covering market-leading EDA, library, IPs, and design service partners.

The TSMC Open Innovation Platform® (OIP) initiative is a comprehensive design technology infrastructure that encompasses all critical IC implementation areas to reduce design barriers and improve first-time silicon success. OIP promotes the speedy implementation of innovation amongst the semiconductor design community and its ecosystem partners with TSMC’s IP, design implementation and DFM capabilities, process technology and backend services.

A key element of OIP is a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that more efficiently empowers innovation throughout the supply chain and, in turn, drives the creation and sharing of newly created revenue and profits. TSMC’s Active Accuracy Assurance (AAA) initiative is critical to OIP, providing the accuracy and quality required by the ecosystem interfaces and collaborative components.

TSMC’s Open Innovation model brings together the innovative thinking of customers and partners under the common goal of shortening design time, minimizing time-to-volume and speeding time-to-market and, ultimately, time-to-revenue. It features:

- The foundry segment’s earliest and most comprehensive EDA certification program delivering timely design tool enhancement required by new process technologies; and
- The foundry segment’s largest, most comprehensive and robust silicon-proven intellectual properties (IPs) and library portfolio; and
- Comprehensive design ecosystem alliance programs covering market-leading EDA, library, IPs, and design service partners.
TSMC’s OIP Alliance consists of 28 electronic design automation (EDA) partners, 41 IP partners, and 25 design service partners. TSMC and its partners proactively work together, and engage much earlier and deeper than before in order to address mounting design challenges at advanced technology nodes. Through this early and intensive collaboration effort, TSMC OIP is able to deliver the needed design infrastructure with timely enhancement of EDA tools, early availability of critical IPs, and quality design services when customers need them. This is critical to success for the customers to take full advantage of the process technologies once they reach production-ready maturity.

In October 2013, TSMC hosted an OIP Ecosystem Forum at the San Jose Convention Center in California, with keynote addresses from TSMC executives as well as OIP ecosystem partners. The forum was well attended by both customers and ecosystem partners and demonstrated the value of collaboration through OIP to nurture innovations.

TSMC’s OIP Partner Management Portal facilitates communication with our ecosystem partners for efficient business productivity. This portal is designed with an intuitive interface and can be linked directly from TSMC-Online.

TSMC University Collaboration Programs

TSMC University Research Centers in Taiwan

TSMC has significantly expanded its interaction with universities in Taiwan with the establishment of several new research centers located at the nation’s most prestigious universities. The mission of these centers is twofold: to increase the number of highly qualified students who are suitable for employment at TSMC, and to inspire university professors to initiate research programs that focus on the frontiers of semiconductor device, process and materials technology; semiconductor manufacturing and engineering science; and specialty technologies of relevance to the semiconductor industry. Two of these research centers were established in 2013 at National Taiwan University and National Chiao Tung University, and two additional centers will be established at National Cheng Kung University and National Tsing Hua University in 2014. These centers are funded jointly by governmental agencies together with a commitment from TSMC of several hundred million Taiwan dollars and in-kind university shuttles. In 2013, about 300 high caliber students across Electronics, Physics, Materials Engineering, Chemistry, Chemical Engineering and Mechanical Engineering disciplines joined these research centers.

A Vehicle to Make Ideas Come True – TSMC University Shuttle Program

The TSMC University Shuttle Program was established to provide professors at leading research universities worldwide with access to the advanced silicon process technologies that are needed to research and develop innovative circuit design concepts. This program links motivated professors and graduate students with enthusiastic managers at TSMC with the goals of promoting excellence in the development of advanced silicon design technologies, and the nurturing of new generations of engineering talent in the semiconductor field.

The program provides access to silicon process technologies including the 65nm and 40nm nodes for digital, analog/ mixed-signal circuits and RF design, and the 0.11µm/0.16µm process nodes for micro-electromechanical system designs. Select research projects utilize the 28nm technology node. Participants in the TSMC University Shuttle Program include major university research groups in the United States: M.I.T.; Stanford University; UC Berkeley; UCLA; University of Texas at Austin; and University of Michigan. In Taiwan, participants are: National Taiwan University; National Chiao-Tung University; and National Tsing-Hua University. Other participants include: Tsing-Hua University in Beijing; Hong Kong University of Science and Technology; and Singapore’s Nanyang Technological University.

TSMC’s University Shuttle Program university participants recognize the importance of the program in allowing their graduate students to implement exciting designs ranging from: low-power memories; analog-to-digital converters; and advanced radio-frequency and mixed-signal biomedical systems. This is truly a “win-win” collaboration. In 2013, TSMC received specific letters of appreciation from professors at M.I.T., Stanford University, UC Berkeley, UCLA, University of Michigan, National Taiwan University and National Chiao-Tung University.
2.2.5 Future R&D Plans

In light of the significant accomplishments of TSMC’s advanced technologies in 2013, the Company plans to continue to grow its R&D investments. The Company plans to reinforce its exploratory development work on new transistors and technologies, such as 3D structures, strained-layer CMOS, high mobility materials and novel 3D IC devices. These studies of the fundamental physics of nanometer CMOS transistors are core aspects of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to ensure our continued industry leadership at the 28nm and 20nm nodes and to extend our leadership to the 10nm and 7nm nodes. One of TSMC’s goals is to extend Moore’s Law through both innovative in-house work and by collaborating with industry leaders and academia. We seek to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC R&D Future Major Project Summary

<table>
<thead>
<tr>
<th>Project Name</th>
<th>Description</th>
<th>Risk Production (Estimated Target Schedule)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10nm logic platform technology and applications</td>
<td>3rd generation FinFET technology for both digital and analog products</td>
<td>2015</td>
</tr>
<tr>
<td>7nm logic platform technology and applications</td>
<td>CMOS platform technology for SoC</td>
<td>2017</td>
</tr>
<tr>
<td>3D IC</td>
<td>Cost-effective solution with better form factor and performance for SIP</td>
<td>2014 – 2016</td>
</tr>
<tr>
<td>Next-generation lithography</td>
<td>EUV and multiple e-beam to extend Moore’s Law</td>
<td>2014 – 2019</td>
</tr>
<tr>
<td>Long-term research</td>
<td>Special SoC technology (including new NVM, MEMS, RF, analog) and 5nm transistors</td>
<td>2014 – 2019</td>
</tr>
</tbody>
</table>

Note: The above plans accounted for roughly 70% of the total R&D budget in 2014. The total R&D budget is currently estimated to be around 8% of 2014 revenue.

2.3 Proprietary Information Protection

We understand the critical value of proprietary information and how crucial it is to safeguard it in order to protect our company’s competitive advantages. Therefore, we established a Proprietary Information Protection (PIP) Program, which governs how proprietary information (including trade secrets, intellectual property, etc) will be protected to preserve the best interests of our company, our shareholders, our customers, our suppliers, and our employees.

Different approaches are adopted to ensure our proprietary information is adequately and effectively protected as described below.

- Security and surveillance systems are used to continuously monitor and control access of personnel and vehicles in and out of our company’s premises. More importantly, these systems help to prevent prohibited items from being used to smuggle any proprietary information out of the premises.
- PIP-related messages are promoted to all employees on a regular basis; we also gather feedback, offer online training courses, and conduct internal compliance checks. This helps to maintain appropriate behavior from top level management down to every single individual employee.
- Severe PIP violations reported will be treated seriously and handled appropriately. Severe violators can face termination of employment and even legal actions.
- We regard our suppliers as our partners, and thus provide security training and management to help them fit in our security management policy. Each individual supplier must take PIP and work safety training, sign a nondisclosure
agreement, and pass the PIP and work safety exam before receiving a working badge. We also hosted a security symposium for suppliers to share successful experiences and review improvement plans. This symposium successfully helped our suppliers to follow our PIP regulations.

As a whole, the scope of PIP program can be summarized as follows:

- Established PIP policies
- Defined PIP management procedures and guidelines
- Implementation physical security measures and controls for PIP
- Leveraging IT security capabilities to deploy innovative PIP solutions
- Providing mandatory PIP training
- Promoting PIP best practices
- Conducting internal compliance checks
- Rewarding PIP-related innovations
- Dealing with PIP violation incidents

We will continuously seek practical ways to better protect our proprietary information.

2.4 Membership in Industry Associations

As a semiconductor industry leader, TSMC actively participates in trade and industry associations. TSMC executives have been nominated to and held senior positions in associations including the Taiwan Semiconductor Industry Association, the Association of Industries in Science Parks, the Chinese National Association of Industry and Commerce, the Taiwan Electrical and Electronic Manufacturers’ Association, the Mount Jade Science and Technology Association of Taiwan, and the Taiwan Business Council for Sustainable Development, holding positions such as Chairman or Executive Board Director. In addition, many TSMC employees also contribute to the semiconductor industry and professional associations by serving in industry associations as committee chairman or vice chairman in various committees.

2.5 Investor Engagement

TSMC’s business strategies and financial policies aim to uphold and increase shareholder value. We align ourselves with international standards that demonstrate our position and reputation as a sustainability champion. In 2013, TSMC was recognized by the Dow Jones Sustainability Indexes (DJSI) as the Semiconductors and Semiconductor Equipment Industry Group Leader, setting a milestone for the Company’s achievements in sustainability and corporate social responsibility.

TSMC is the first Taiwan company, and one of just four Asian companies, to win the highest score out of its industry peers in the DJSI’s 24 industry groups, made up of 59 industries and 2,500 largest companies in the world. Moreover, TSMC is one of only two semiconductor companies chosen as index components for 13 consecutive years. Of the Semiconductor and Semiconductor Equipment Industry Group companies, TSMC scored highest in categories including Supply Chain Management, Environmental Policy and Management.
Since becoming a publicly listed company in 1994, TSMC has consistently delivered value to shareholders through cash dividends and share price appreciation, maintaining a strong balance sheet, and keeping one of the highest credit ratings among global semiconductor companies and Taiwan companies (Standard & Poor’s (S&P) Ratings: A+; Moody’s Ratings: A1; Taiwan Ratings: twAAA). In our core semiconductor business, we invest in opportunities that will expand our leadership in technology and capacity. In 2013, in addition to a record R&D budget of US$1.6 billion, TSMC spent an unprecedented US$9.7 billion on capital expenditures to meet the capacity needs of our customers. Moreover, we actively pursue new revenue opportunities in solid state lighting and thin film solar photovoltaic technology, which leverage our technological strengths and engineering capabilities. We believe these investments will fuel TSMC’s future growth and maximize our shareholder value.

In order to serve investors and the investment community, TSMC has established a highly effective communication system to disseminate information. Each quarter, our CEO and CFO jointly hold an earnings conference, which combines face-to-face interactions with an audio conference call, to report and discuss company performance with investors worldwide. Replays and transcripts of these conferences are then made available on the Company website for investors’ reference. Each year, our Investor Relations team holds hundreds of investor meetings.

Note: TSMC prepared 2004-2011 financial performance in accordance with R.O.C. GAAP.
and analyst meetings and conference calls, and actively participates in broker-sponsored investor conferences and non-deal roadshows, extending our reach throughout Asia, Europe and North America. In 2013, more than 260 such meetings and conference calls were held with investors worldwide. All these efforts are focused on serving worldwide investors with accurate, timely, and transparent information and financial data regarding TSMC business strategy, operations and performance. In addition, E-mail updates covering all business activities and key events are regularly sent to thousands of members of the investment community. Information regarding TSMC’s business fundamentals, summaries of analysts’ recommendations, credit ratings, and important filings with regulatory authorities are posted on TSMC’s corporate website in a timely manner.

In order to increase shareholder value, TSMC has established clear strategic financial objectives. These strategic financial objectives include: (1) average return on equity (ROE) across cycle greater or equal to 20%; (2) 10% compounded annual growth rate (CAGR) for profit before tax (PBT) from 2010 to 2015. These financial objectives can help investors better understand TSMC’s long-term investment value, while our financial track record gives investors higher confidence in TSMC’s capability to achieve these financial objectives. For example, during the past 10 years, TSMC’s averaged ROE was 24% and CAGR for profit before tax was 15%, both of which met our long-term financial objectives. Supported by solid financial performances, TSMC’s share performance including cash dividends increased 12% during 2013, marking five consecutive years of annual growth. Since the Company went public in 1994, TSMC’s market capitalization has grown steadily. As of December 31, 2013, TSMC’s market capitalization reached above NT$2.7 trillion, or US$91 billion.

Annual investors’ surveys conducted by media have recognized the transparency of TSMC’s disclosure policies, corporate governance commitment, and equitable treatment of shareholders. Furthermore, in 2013, TSMC continued to receive various awards from globally noted institutions such as Institutional Investor and IR Magazine. For more information on awards and recognition in 2013, please refer to “2013 Awards and Recognitions” on page 6.

### 2.6 Financial Highlights

#### Dividend Policy

TSMC’s profits may be distributed by way of cash dividend and/or stock dividend. The preferred method of distributing profits is by way of an annual cash dividend. Under TSMC’s Articles of Incorporation, stock dividends shall not exceed 50% of the total dividend distribution in any given fiscal year. TSMC does not pay dividends when there is no profit or retained earnings. TSMC has distributed cash dividends every year to its shareholders since 2004 and maintained dividends retained earnings. TSMC has distributed cash dividends every year to its shareholders since 2004 and maintained dividends per share (DPS) at NT$3.0 every year since 2007. TSMC intends to maintain a stable dividend policy, and will consider raising DPS when the free cash flow significantly exceeds NT$3.0 per share.

For 2012 earning distribution, TSMC paid dividends of NT$3.0 in cash per common share in 2013.

#### Tax Policy

TSMC supports tax policies and incentives that encourage innovation and foster economic growth. In R.O.C., such policies include measures that enable companies to compete globally and incentivize research and development activities.

TSMC’s payments to the governments are primarily for corporate income tax. In 2013, TSMC paid a total of corporate income tax at NT$14.5 billions, over 90% of which was paid to the Taiwan R.O.C. government, and was the largest corporate taxpayer in the main country of our operations.

Based on previous expansion, the purchase of production equipment and research and development expenditures, TSMC was entitled to tax incentives such as tax exemption and investment tax credits in 2013 as follows:

<table>
<thead>
<tr>
<th>Law/Statute Item</th>
<th>Item</th>
<th>(In Billions of NTS)</th>
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</thead>
<tbody>
<tr>
<td>Article 9 of the Statute for Upgrading Industries</td>
<td>5-year tax exemption</td>
<td>8.6</td>
</tr>
<tr>
<td>Article 6 of the Statute for Upgrading Industries</td>
<td>Purchase of machinery and equipment</td>
<td>4.8</td>
</tr>
<tr>
<td>Article 6 of the Statute for Upgrading Industries</td>
<td>R&amp;D and personnel training expenditures</td>
<td>4.0</td>
</tr>
<tr>
<td>Article 10 of the Statute for Industrial Innovation</td>
<td>R&amp;D expenditures</td>
<td>3.1</td>
</tr>
</tbody>
</table>
2.5  Investor Engagement  
2.4  Membership in Industry Associations 
2.3  Proprietary Information 
2.2  Innovation Management 
2.1  Market/Business Summary

Capital and R&D Expenditures

<table>
<thead>
<tr>
<th>Year</th>
<th>Capital Expenditures</th>
<th>R&amp;D Expenditures</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>88</td>
<td>22</td>
</tr>
<tr>
<td>2010</td>
<td>187</td>
<td>30</td>
</tr>
<tr>
<td>2011</td>
<td>214</td>
<td>34</td>
</tr>
<tr>
<td>2012</td>
<td>246</td>
<td>40</td>
</tr>
<tr>
<td>2013</td>
<td>288</td>
<td>48</td>
</tr>
</tbody>
</table>

Unit: NTS Billions

Income before Tax and Income Tax Expense

<table>
<thead>
<tr>
<th>Year</th>
<th>Income before Tax</th>
<th>Income Tax Expense</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>95</td>
<td>6</td>
</tr>
<tr>
<td>2010</td>
<td>170</td>
<td>8</td>
</tr>
<tr>
<td>2011</td>
<td>145</td>
<td>11</td>
</tr>
<tr>
<td>2012</td>
<td>162</td>
<td>16</td>
</tr>
<tr>
<td>2013</td>
<td>215</td>
<td>27</td>
</tr>
</tbody>
</table>

Unit: NTS Billions

Assets and Capitalization – Year End

<table>
<thead>
<tr>
<th>Year</th>
<th>Total Assets</th>
<th>Stockholders' Equity</th>
<th>Weighted Average Diluted Shares Outstanding</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>495</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>579</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>632</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td>723</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td>848</td>
<td>29</td>
<td></td>
</tr>
</tbody>
</table>

Unit: NTS Billions

Dividends Distribution

<table>
<thead>
<tr>
<th>Year</th>
<th>Dividends Distribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>3.00</td>
</tr>
<tr>
<td>2010</td>
<td>3.00</td>
</tr>
<tr>
<td>2011</td>
<td>3.00</td>
</tr>
<tr>
<td>2012</td>
<td>3.00</td>
</tr>
<tr>
<td>2013</td>
<td>3.00</td>
</tr>
</tbody>
</table>

Unit: NTS

Revenue and Net Income

<table>
<thead>
<tr>
<th>Year</th>
<th>Revenue</th>
<th>Net Income (shareholders of the parent)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>209</td>
<td>89</td>
</tr>
<tr>
<td>2010</td>
<td>429</td>
<td>162</td>
</tr>
<tr>
<td>2011</td>
<td>427</td>
<td>134</td>
</tr>
<tr>
<td>2012</td>
<td>507</td>
<td>166</td>
</tr>
<tr>
<td>2013</td>
<td>597</td>
<td>188</td>
</tr>
</tbody>
</table>

Unit: NTS Billions

Note: TSMC prepared 2009-2011 financial performance in accordance with R.O.C. GAAP.