

Circuit-under-Pad (CUP) I/Os



Reference Flow

Process-Optimized Technology Files



90nm



Chip Implementation Services



Libraries



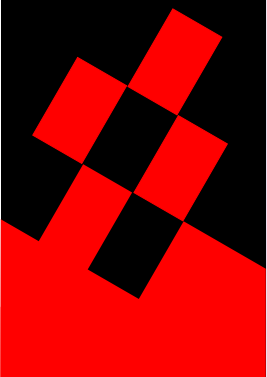
Customization Services

IP

Multiple Vt

TSMC's

Integrated Design Infrastructure



Fast Time-To-Volume

Improving Your Time-to-volume, Especially for Advanced Technology Designs ...

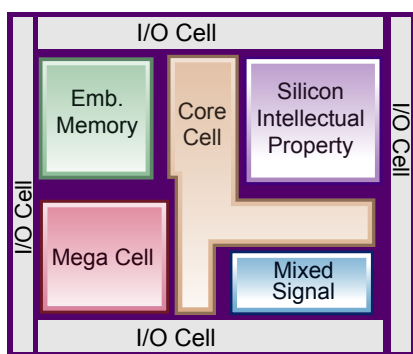
... that's the single mission of TSMC's Integrated Design Infrastructure. What is a Design Infrastructure? It is an integrated portfolio of products and services targeted to advanced process technologies at 0.18-micron and below. TSMC's Design Infrastructure provides another choice to empower design innovation and to enhance design-for-manufacturability in this less-than-perfect design world.

TSMC's Integrated Design Infrastructure is the only one of its kind in the foundry industry. It has been developed by TSMC's Design Services Division (DSD) who are an essential part of the TSMC R&D team for advanced technology development. Over the years, DSD has specialized in developing sound silicon validation procedures, process-optimization approaches, and design-for-manufacturability (DFM) methodologies. This expertise has led to a high quality design infrastructure, including libraries and intellectual property (IP), technology files, reference design flows and chip implementation services. In addition, DSD provides engineering services such as library and IP customization, and design consulting.

Empowering InnovationSM

As advanced designs migrate to smaller and smaller geometries, selecting just the right library, IP or technology file has become an increasingly daunting task. That's why TSMC is now offering its in-house silicon-verified libraries and advanced silicon IP at 0.15-micron and below. This new and expanding portfolio provides today's SoC designers with a quality choice to empower design innovation.

- **TSMC Libraries** -- TSMC offers a wide spectrum of silicon-proven and process-optimized standard cell and I/O libraries for TSMC's advanced process technologies. These libraries were developed in parallel with each advanced process technology node. As a result, the standard cell libraries have achieved the highest density without any compromise to manufacturing. The new multiple-Vt library option adds design flexibility which further enables the best possible speed and power optimization. TSMC I/O libraries have enabled more than 200 first-pass silicon successes with outstanding performance. Both standard cell and I/O libraries are now available for TSMC 90-nanometer, 0.13-micron and 0.15-micron process technology families.



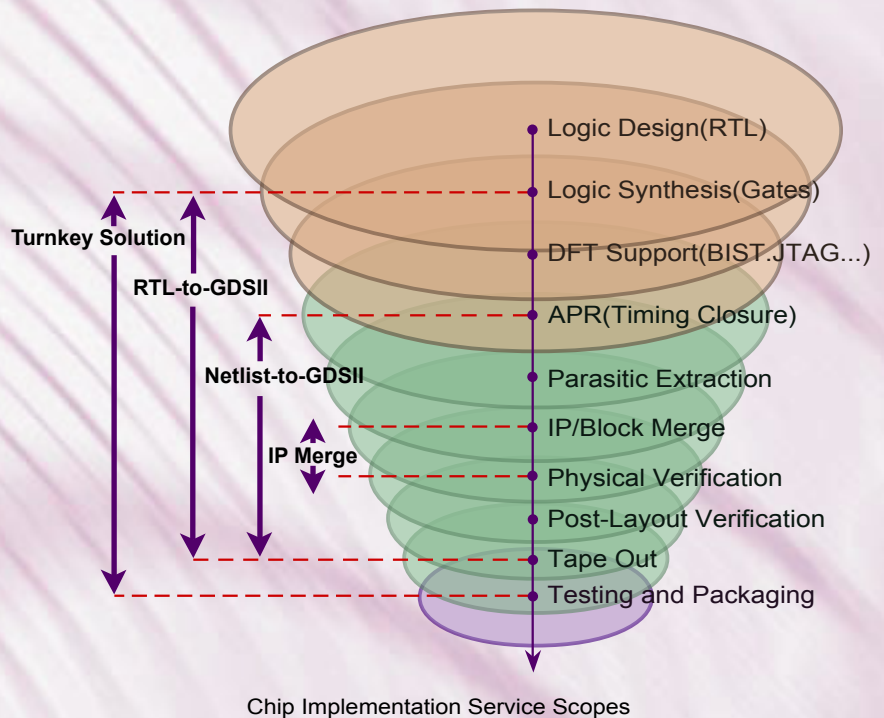
- **TSMC IP** -- TSMC in-house IP portfolio is an integral part of TSMC's industry-leading IP catalog that includes a large collection from its third-party IP Alliance partners. TSMC's in-house IP focuses on silicon-dependent IP for advanced technologies. The IP portfolio includes mixed-signal, RF, embedded memory macros and specialty I/O. The specialty I/O portfolio covers most of the industry standard-based I/Os such as USB SSTL, LVDS, HSTL and SerDes. The mixed-signal/RF product line includes silicon-proven PLL, DAC, ADC and RF front-ends for advanced process technologies. Embedded memory macros include SRAM, high-density 1TRAM and non-volatile FLASH optimized for each unique SoC design requirement.

- **Chip Implementation Services** -- TSMC's chip implementation services leverage many years of experience in internal design infrastructure development and contract services. Chip implementation services provide RTL-to-GDSII, Netlist-to-GDSII and Netlist sign-off services to facilitate migration to Customer-Owned Tooling (COT) and to shorten time-to-tapeout. Chip implementation services, although available for all technologies, are strategically focused on TSMC's 90-nanometer and 0.13-micron process technologies.

Design-For-Manufacturability

Companies engaged in today's complex advanced technology SoC designs have reached the conclusion that design-for-manufacturability is one of the key elements of successful time-to-volume and time-to-revenue. TSMC's Integrated Design Infrastructure includes a portfolio of design-for-manufacturability services that are accessible through TSMC-Online.

Reference Flow -- TSMC's reference design flow, currently in its third generation, is the foundry industry's first manufacturing-centric IC design flow. DSD engineers anticipate future design and manufacturing challenges associated with the advanced technologies then collaborate with industry's best engineering talent to develop the most optimum design flows. The reference design flows provide sophisticated and well-documented design implementation methodologies that significantly improve design quality and productivity as well as providing the best possible manufacturability of your SoC design. These multi-generation reference flows have been proven to reduce time-to-volume and to save design costs.



Technology Files -- DSD engineers have developed high accuracy technology files - from design rule checking (DRC), interconnect resistance and capacitance extraction (RCX) to layout-vs.-schematic (LVS) command files - for the worlds' major EDA tools. They go the extra mile to ensure design accuracy and to reduce the number of design iterations through careful calibration and validation of technology files down to the silicon level. This has contributed to a large number of first silicon successes.

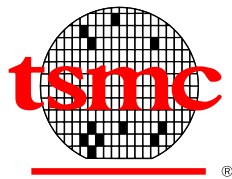
And There's More

DSD continues to add innovative services and products to TSMC's Integrated Design Infrastructure.

Customization Services -- The foundry business is, by nature, tailored to customers' needs. And this same customization applies to TSMC's Integrated Design Infrastructure. Along with design consulting, DSD offers a wide range of customization services for libraries, silicon IP, reference flows and technology files that meets your specific design requirements and design schedule.

New Developments -- Here's a short list of projects that DSD is currently working on that will pay future dividends for you:

- 90 nm SoC readiness: This project is designed to enhance the current baseline offering of complete libraries, silicon IP, memory macros and technology files with advanced reference flows and power/performance management schemes.
- Circuit-under-Pad (CUP) I/Os: By folding pads onto the I/O cell area, CUP I/Os can save valuable silicon area and die costs. TSMC is conducting extensive functional and reliability evaluation at the silicon and package levels for TSMC's 0.18-micron, 0.13-micron technologies and, later on, for 90-nanometer technologies.
- Flip-Chip Solution: The project expands the current Re-Distribution Layer (RDL) design flow to a ground-up or area array flow to further reduce die size and improve design flexibility.



Empowering Innovation

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