Technology Leadership

1. R&D Organization and Investment

TSMC increased its research and development investment and expanded its world-class R&D organization in 2006 to provide best-in-class semiconductor technologies and design solutions to our customers. R&D expenditure reached NT$14.6 billion, while R&D staff grew by 13.5 percent during the same period. We plan to continue to invest significant amounts on research and development in 2007, with the goal of maintaining a leading position in the development of advanced process technologies. TSMC also strengthened the capabilities and expanded the capacity of our 300mm R&D pilot line for advanced process development in 2006 to accommodate our growing R&D development activities.

TSMC continued to accelerate the development of transistor, memory, and interconnect technologies. During 2006, the R&D organization was reorganized into exploratory research and platform development organizations to better support TSMC’s technology development. We also expanded our external R&D partnership and alliance activities with tool and materials vendors. For example, TSMC is a core member of IMEC, a world-class CMOS R&D consortium in Europe. In addition, TSMC and Freescale completed joint development of cutting edge 65 nanometer SOI technology. TSMC also strengthened its collaborative research effort with key partners for design-process co-optimization, which enables the best technology and design solutions for product success in the complex and challenging nanometer era. Since 2001, TSMC has been funding nanotechnology research at major universities worldwide to promote innovation and the advancement of technology.

2. R&D Accomplishments in 2006

2.1 R&D Highlights

Sixty-five Nanometer Technology

TSMC was the first foundry to qualify production-ready 65 nanometer technology in 2006, beginning with low-power process technology. We continued to expand our 65 nanometer portfolio, successfully completing technology qualification and customer product pilot runs for various technology families including general purpose and triple gate oxide processes.

TSMC’s 65 nanometer technology is the company’s third-generation semiconductor process employing both copper interconnects and low-k dielectrics. It is a nine-layer metal process with core voltages of 1.0 or 1.2 volts, and I/O voltages of 1.8, 2.5 or 3.3 volts. The new technology offering supports a standard cell gate density twice that of TSMC’s 90 nanometer process.

Sixty-five Nanometer Embedded DRAM

TSMC developed the foundry sector’s first functional 65 nanometer embedded DRAM customer product in 2006. TSMC’s 65 nanometer embedded DRAM features improved retention time and a low thermal budget module that can be added to the company’s standard CMOS process. It is compatible with all 65 nanometer logic libraries making it an efficient process for IP reuse. The process also offers special power saving features for low power applications including sleep mode, partial power cut-off and on-chip temperature compensation.

The 65nm embedded DRAM process is built on up to 10 metal layers using copper low-k interconnect and nickel silicide transistor interconnect. It features a cell size less than a quarter of its 90nm counterpart, and macro densities ranging from 4Mbits to 256Mbits.

65nm Technology Qualified and Production-ready in 2006: First in Foundry

Immersion Lithography

TSMC’s immersion lithography program used proprietary techniques to produce nearly defect-free test wafers well within acceptable parameters for volume manufacturing. On initial tests, TSMC’s techniques produced less than seven immersion-induced defects on many 12-inch wafers, a defect density of 0.014/cm². Some wafers have yielded defects as low as three per wafer, or 0.006/cm². This compares to several hundred thousand defects produced by a prototype immersion scanner without these proprietary techniques and is significantly better than published champion data in double digits.

TSMC is now focusing on throughput improvement for high-volume manufacturing and cooperating with equipment manufacturers to develop production-ready immersion lithography equipment. TSMC’s immersion lithography technology is targeted at our 45 nanometer manufacturing process.

Forty-five Nanometer Technology

TSMC’s 45 nanometer technology development made a strong start in 2006. Our test vehicles achieved defect densities of less than 10 per wafer by the end of the year, reaching this important milestone two quarters earlier compared with our 65 nanometer technology development timeline.

Our 45 nanometer technology development also highlights the intimate collaboration between manufacturing and design at this advanced technology node. Having made substantial progress in technology development, we were able to offer our first 45 nanometer low-power design verification shuttle in 2006. This shuttle was the foundry industry’s first 45 nanometer design verification shuttle and also the earliest shuttle compared with TSMC’s past technology generations. TSMC expects to begin risk production of 45 nanometer technology in the second half of 2007.

2.2 Spectrum of Technologies

In addition to the highlights above, TSMC continued to introduce a rich mix of new technologies. For example:

Mixed Signal/Radio Frequency Technology

TSMC developed and qualified mixed signal/radio frequency (MS/RF) technologies at both 90 nanometer and 65 nanometer generations. The technologies feature a 2.0fF/µm² high-density Metal-insulator-Metal (MIM) capacitor, a 3.3 micron Ultra Thick Metal (UTM) for high quality inductor, and a patented Kaleidoscopic Metal-Over-Metal (K-MOM) capacitor with a greatly improved mismatch compared with traditional MOMs.
Silicon Germanium BiCMOS Technology
TSMC developed a high-voltage version of 0.18 micron Silicon Germanium (SiGe) BiCMOS technology to serve the needs of power amplifier product customers. TSMC’s 0.18 micron SiGe technology enables high performance power amplifier applications and provides an integrated solution that is more cost effective compared to GaAs technology.

CMOS Image Sensor Technology
Following the successful mass production of 0.13 micron 4T CMOS image sensors, TSMC developed a high-performance and low-cost 0.11 micron 4T CMOS image sensor process with AlCu backend. This new process is aimed at high-end imaging applications with small pixel size of 1.75 micron and high resolutions of greater than three megapixels. It is compatible with TSMC’s 0.13 micron CMOS logic and embedded memory processes, enabling System-on-Chip (SoC) platforms for consumer and industrial applications in mobile phones, digital cameras, security sensors and other image sensor markets.

45nm Design Verification Shuttle: First in Foundry

Flash/Embedded Flash Technology
TSMC demonstrated excellent intrinsic reliability data for automotive applications using flash/embedded flash technology at the 0.18 micron technology node. Our test vehicles achieved very low failure rates for both cycling test and data retention after a bake at 250 degree Celsius. In addition, a programmable fuse IP has been verified on silicon for 0.18 micron high voltage technology. We developed and verified IP with read functionality at 3.3 volt and 1.5 volt Vcc for 0.13 micron embedded flash technology, which meets endurance specifications. TSMC also worked out a very competitive split-gate Flash device for 90 nanometer embedded flash. With this new cell architecture, TSMC can continue the scaling trend of split-gate flash at the 90 nanometer node, improving density by four times compared with the 0.18 micron technology node. A test vehicle has been taped out to verify the new flash device.

Mask Technology
Mask technology is an integral part of advanced lithography. TSMC has developed proprietary resolution-enhancement techniques that are closely optimized with our in-house mask-making technology, including optical proximity correction, phase-shifting, and subresolution-assist mask features. In 2006, we popularized fast Lithography Process Check technology, which is a critical element of Design For Manufacturing. TSMC mask facilities feature state-of-the-art E-beam mask writers, etchers, inspection and repair tools for both R&D and production use. TSMC’s strength in mask technology R&D and production provides significant benefits to our customers in terms of technical excellence, quality, fast cycle time, and one-stop service. In 2006, the Company successfully developed high-quality, cost-effective 55 nanometer mask making technology for production, X-metal mask technology, as well as mask technology for the 45 nanometer generation. The Company also developed metrology using e-beam, scatterometry, and electrical techniques to support wafer lithography and mask making.

3. Intellectual Property
A strong portfolio of intellectual property rights strengthens TSMC’s technology leadership. In 2006, TSMC received 470 U.S. patents, 463 Taiwan patents, 143 PRC patents, and other patents around the world. TSMC has been ranked by a Ministry of Economic Affairs Special Project on Technology as the number-one Taiwan company in procuring U.S. patents. We have taken initiatives in building the various elements of a model for TSMC’s intellectual capital management. Management and use of our intellectual property rights are driven by strategic considerations and business objectives.

At TSMC, we have built a process to extract value from our intellectual property rights. Our IP strategy works in conjunction with our R&D, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities. We have worked continuously to improve the quality of our IP portfolio, reduce cost of maintenance, align business strategies with IP strategies, and extract value from our portfolio. IP is an essential element for our ability to attract customers and partners and the basis of collaboration with them. We expect to continue investing in our IP portfolio and the management system to ensure that we receive maximum value from our intellectual property rights.