

5. Operational Highlights

5.1 Business Activities

5.1.1 Business Scope

As the founder and a leader of the dedicated semiconductor foundry segment, TSMC has built its reputation by offering advanced and “More-than-Moore” wafer production processes and unparalleled manufacturing efficiency. TSMC strives to provide the best overall value to its customers, and the success of TSMC’s business is manifested in the success of its customers.

TSMC provides a full range of integrated semiconductor foundry services that fulfill the increasing variety of customer needs. In the process, it has experienced strong growth by building close relationships with customers. Semiconductor suppliers from around the world trust TSMC with their manufacturing needs, thanks to its unique integration of cutting-edge process technologies, pioneering design services, manufacturing productivity and product quality.

In May 2009, TSMC established the New Businesses organization to explore non-foundry related business opportunities. In August 2011, the New Businesses organization was formally separated from the main TSMC organization as two subsidiaries, TSMC Solid State Lighting Ltd. and TSMC Solar Ltd., responsible for solid state lighting and solar business activities, respectively.

5.1.2 Customer Applications

Over the past 25 years, more than 600 customers worldwide have relied on TSMC to manufacture chips that are used across the entire spectrum of electronic applications, including computers and peripherals, information appliances, wired and wireless communications systems, automotive and industrial equipment, consumer electronics such as DVDs, digital TVs, game consoles, digital still cameras (DSCs), and many other applications.

The rapid evolution of end products drives our customers to utilize TSMC’s innovative technologies and services, while at the same time spurring TSMC’s own development of technology. As always, success depends on leading rather than following industry trends.

5.1.3 Unconsolidated Shipments and Gross Sales in 2012 and 2011

Unit: Shipments (8-inch equivalent wafers) / Gross Sales (NT\$ thousands)

		2012		2011	
		Shipments	Gross Sales	Shipments	Gross Sales
Wafer	Domestic	2,348,115	64,958,354	2,077,487	49,039,389
	Export	11,508,104	401,877,584	10,411,227	340,588,566
Package	Domestic	0	0	0	0
	Export	143,267	6,124,451	24,881	1,045,714
Other	Domestic		4,180,117		4,499,828
	Export		29,557,232		26,298,590
Total	Domestic	2,348,115	69,138,471	2,077,487	53,539,217
	Export	11,651,371	437,559,267	10,436,108	367,932,870

5.1.4 Production in 2012 and 2011

Unit: Capacity / Output (8-inch equivalent wafers) / Amount (NT\$ thousands)

Wafers				
Year	Capacity	Output	Amount	
2012	15,090,605	13,875,440	270,740,990	
2011	13,221,316	12,019,882	204,927,905	

5.2 Technology Leadership

5.2.1 R&D Organization and Investment

TSMC further expanded many aspects of Research and Development in 2012 to strengthen Technology Leadership. In 2012, the total R&D budget was 8.0% of total revenue. This level of R&D investment equals or exceeds that of many leading-edge technology companies. Along with the budget increase, the R&D organization increased staffing by over 27.5%.

TSMC recognizes that the technology challenge required to extend

Moore's Law, the business law behind CMOS scaling, is getting increasingly complex. R&D Vice Presidents bring their rich industry experiences to lead the strengthening of the R&D team and to navigate through the technological and competitive challenges ahead. In 2012, TSMC worked intensively on ramping 28nm technology, which contributed close to 22% of fourth quarter 2012 revenue and will further increase in 2013.

TSMC accelerated the development of advanced transistors, especially 3D transistors using FinFET structure for 16nm process node, embedded memories, and copper (Cu)/low-K interconnect technologies. During 2012, the R&D organization once again proved its capabilities by developing 20nm technology as well as establishing 16nm transistor leadership capabilities. Furthermore, TSMC broadened the horizon of transistor research by investing R&D in alternative high-speed and low-power channel materials other than silicon, such as germanium and III-V compounds.

TSMC also expanded its external R&D partnerships and alliances with world-class research institutions. For example, TSMC is a core partner of IMEC in Belgium, the respected European R&D consortium. TSMC also has strategic agreements with IP providers to enable the development of reusable IPs through the advanced technology nodes. TSMC strengthened its collaborations with key development partners on design-process optimization, and provides funding for nanotechnology researches at leading research universities worldwide to promote innovations and the advancement of technology.

These research efforts enable the Company to continuously offer its customers the foundry-leading, first-to-market technologies and design solutions that contribute to their product success in today's complex and challenging market environment.

5.2.2 R&D Accomplishments in 2012

R&D Highlights

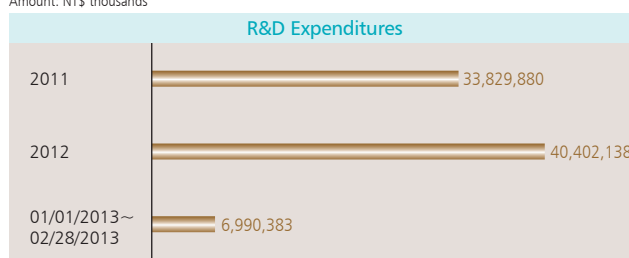
● 28nm Technology

In 2012, TSMC's 28nm technology offering added 28nm High Performance Plus (28HPP) and 28nm High Performance Triple-Gate (28HPT). 28HPP and 28HPT achieved 10% faster speed than that in previous 28nm High Performance (28HP) and 28nm High Performance Mobile Computing (28HPM) offered in 2011. 28HPP was qualified and demonstrated first silicon success in early production. 28HPT received first customer tape out in December 2012, and was scheduled to deliver first silicon success by April 2013.

● 20nm Technology

In 2012, TSMC continued to focus on 20nm technology development, including process baseline setup and yield learning, design rule definition and enhancement, SPICE model generation, and reliability evaluation. To offer a leading-edge technology for both digital and analog applications, the Company adopted an advanced lithography process for smaller feature size. With the second generation of high-K metal-gate, more Si strain, and new device structure, the intrinsic transistor performance continues to enhance following Moore's Law. Meanwhile, external resistance can be effectively reduced and controlled by a specially designed process technique. The back-end-of-line (BEOL) interconnect process

Amount: NT\$ thousands



features extreme low-K inter-metal dielectric materials and copper metallization with the novel low-resistance scheme. The logic transistor and SRAM bit-cell offering, using the 20nm process, can satisfy high performance System-on-Chip (SoC) applications.

Development of 20nm technology will create superior gate density and chip performance. The cost and complexity of advanced technology will continue to escalate for customers. In 2012, TSMC successfully taped out the process development test vehicle, defect reduction vehicle and product-like yield learning vehicle, on which the advanced ARM-core block was included. With the vehicle and process development, TSMC provided V1.0 process flow, design kits (design rules, SPICE models, and PDK files) and intellectual property (IP) to help reduce foundry-access costs in 2012. The Company achieved its outstanding transistor performance target and demonstrated the functional and natural yield of the leading-edge SRAM bit-cells as planned. Besides the internal test vehicles, the Company also launched two public cyber shuttles in April and November 2012. More than 10 customers took the shuttles and verified their IPs. TSMC's high-performance 20nm process enters risk production in first quarter of 2013.

● 16nm Technology

TSMC completed 16nm technology definition and began 16nm technology development in 2012. In order to further extend Moore's Law, the FinFET transistor, an advanced 3D device structure, was introduced in the 16nm technology in addition to the third generation of high-K metal gate, the fifth generation of strain technology and advanced 193nm lithography. As a result, the 16nm technology offers substantial power reduction for the same chip performance, a must for advanced mobile applications as compared to technologies built with the traditional planar structure.

In 2012, TSMC achieved significant progress on test vehicle generation, process baseline setup, design rule definition, SPICE model generation and reliability evaluation. TSMC successfully taped out a process development test vehicle, provided customers early design kits (design rules and SPICE models) and demonstrated functional yield on the FinFET-based SRAM bit-cells according to plan.

● Lithography

20nm lithography progressed steadily in 2012. There has been continuous learning and improvement in material quality, process recipe robustness, and litho-cell maintenance that resulted in robust patterning solutions. The achieved defect learning and D0 goals enable successful yield learning on SRAM qualification vehicles and several key customer tape-outs.

Lithography for the 16nm node signifies the introduction of novel patterning techniques to achieve 48nm pitch FinFET, especially to ensure sufficient coverage and planarization of high aspect ratio

topography with the 3D device structures. In addition, TSMC has also developed the patterning solution to delineate the tightest single patterning pitch of 80nm for the metal layer enabling further increase of pattern density for customers. Building on the learning of the 20nm node, TSMC has automated the in-line pilot run process and its control that enable fast cycle time for SRAM development and yield learning.

The pathfinding for 10nm node has been started on immersion scanners. This technology will become more sophisticated and play a key role as the process baseline, based on considerations of cost and next-generation tool availability. Innovative processes are being developed to deal with the process control challenges brought with this technology node. Optical proximity correction has solved the process problem. Both cost and measurement accuracy were greatly improved with this change.

Development of EUV lithography and multiple e-beam direct write is aimed at the 7nm node because of late availability. Nevertheless, the 10nm node will be used to exercise these technologies.

At the front of specialty technology, R&D lithography has further extended the limitation of scanners in the 8-inch fabs, to shrink the design rules and help customers gain more gross dies per wafer to reduce the die cost. R&D has transferred multiple eFlash technologies for manufacturing and delivered eMRAM and eRRAM lithography technologies. For MEMS, R&D has developed and transferred the manufacturing technology for microphones and accelerometers.

TSMC continues to work with exposure-tool partner ASML in the development of immersion and EUV lithographic technologies. Faced with delays in the EUV source technology, capabilities of 193nm immersion scanners are being extended with more resolution-enhancement features, tighter specifications, and higher throughput to enable multiple patterning. In the meantime, using NXE3100 beta-tool in Fab 12, we have been developing single-patterning EUV processes for 10nm and 7nm applications, with associated mask and resist technologies. However, the application of EUV lithography in high-volume manufacturing of these nodes will depend on the success of the EUV source technology to reach over 100 wafers per hour.

The KLA-Tencor REBL multiple-e-beam direct-write tool is being extensively studied for feasibility, performance, and improvements. A TSMC team from the design, CMOS, MEMS, and packaging areas is jointly developing and fabricating the dynamic pattern generation chip for the REBL system. Two test stands for qualification of dynamic pattern generation and resist testing are being built and will be delivered to the TSMC Fab 12 GIGAFAB™ facility in 2013. Two scanner companies are performing sizing feasibility for multiple e-beam direct-write lithography. Multiple e-beam direct-write

lithography not only has the potential for imaging critical layers, it also offers cost reduction potential for non-critical layers and 450mm wafers.

● Mask Technology

Mask technology is an integral part of advanced lithography technology. In 2012, TSMC completed the development of the mask technology for the 20nm node to enable double patterning. TSMC's R&D mask facility received more state-of-the-art mask processing tools to enable engineers to complete the development of mask technologies for the 16nm and 10nm nodes in the coming years. Development of mask technology for EUV lithography has been underway with its unique requirements in e-beam writing, etching, inspection, repair, and verification. As a core member of SEMATECH and a joint-development partner of EIDEC, TSMC is an active participant in the development of key infrastructure pieces for EUV masks such as the actinic repair verification tool and the actinic inspection tool of EUV blanks.

Integrated Interconnect and Packaging

In 2012, TSMC became the world's first foundry to provide full system integration turn-key solutions to customers. The Company developed and delivered backend technologies starting from advanced back-end-of-line (BEOL) interconnect, to the production-ready fine pitch silicon interposer with through silicon via (TSV) & chip stacking, and all the way to the advanced wafer-level-chip scale packaging (WLCSPP) including fan-in and fan-out, and ultra fine pitch large die lead-free flip chip packaging. TSMC can offer our customers corresponding design tools, technology and mass production capability. Such options were made available to customers in 2012. Advanced BEOL interconnection is further refined and extended with innovative damascene processes. And the flip chip packaging technology envelope was expanded to larger chip size and finer bump pitches for advanced technology nodes (28nm and 20nm). Efforts are also made to include fan-in and fan-out wafer level packaging technology in our offerings to customers. The solution has been qualified by selective customers.

● Advanced Interconnect

Advanced interconnects with low resistance/capacitance RC delay continued to be the primary focus of TSMC BEOL technology development in 2012. For 16nm node and beyond, we have developed a new interconnect scheme to achieve minimum pitch and a new metal patterning to minimize resistance/capacitance RC delay.

At the 20nm node, the effective resistivity of our Cu lines is highly competitive and lower than that projected by the International Technology Roadmap for Semiconductors (ITRS).

● Advanced Package Development

To provide innovative and cost competitive lead-free bumping and packaging solutions in 2012, TSMC developed and qualified 28nm technology node Bump-on-Trace packaging technology with ultra-fine pitch array (100 μ m pitch) Cu-bump for mobile devices. The Company expanded the lead-free packaging technology envelope to 20nm node and offered a wide variety of lead-free flip chip packaging technologies for both mobile/handheld and high performance applications to enhance customers' competitiveness.

● 3D IC

In 2012, R&D completed CoWoS™ process and package qualifications and transferred the technology for production. CoWoS™ solution provides a simple integration process for customers to realize their products with the optimized cost and cycle time. We have also developed the 3D IC 28HPM through transistor stacking (TTS) technology, that can enable customers for applications requiring small form factor, high performance and low power dissipation. Realizing the critical nature of 3D IC thermal management, TSMC has also developed thermal solutions associated with the CoWoS™ process and TTS technologies. Overall, TSMC delivers technology solutions to enable SiP design that includes package design, electrical analysis of package extraction, timing, signal integrity, IR drop, and thermal to physical verification of design rule check (DRC) and layout verification of schematic (LVS). Such integrated solution for product realization is available to customers.

Advanced Transistor Research

Continuous quest for high performance and low power drives innovation and research in transistor architecture in advanced logic technologies across all segments. TSMC invested heavily in alternative high speed and low power channel materials other than silicon, such as germanium and III-V compounds. New concepts of transistor structures employing innovative nanotechnology are also under intensive investigation.

Spectrum of Technology

In addition to CMOS logic technology, TSMC continues to conduct research and development on a broad mix of capabilities. The Company enhanced its SoC roadmap, with higher integration and more variants.

● Mixed Signal/Radio Frequency (MS/RF) Technology

TSMC developed full scope 28nm oxi-nitride and poly-Si based RFCMOS technology for next generation RF transceivers (ex. 4G LTE) with the advantages of low power & low cost. Besides standard-Vt and low-Vt devices, extreme-low-Vt devices were also included for larger design margins and smaller active-power consumption. TSMC delivered a CMOS process compatible technology for enabling cellular RF switch applications on Si to compete with traditional compound

semiconductor-based process. TSMC enabled production of the IPD (Integrated Passive Device) technology, specifically for rapidly expanding mobile devices.

● Power IC/BCD Technology

In 2012, TSMC's HV/ Power technologies collectively shipped more than 1 million wafers to customers. On top of the production base, R&D team released the second generation of 0.18 BCD technology, and the first product from a partner customer has shipped engineering samples to system customer.

● Panel Driver Technology

In 2012, 80HV for smartphone display driver chips was released to production. And a customized derivative of the technology has also supported partner customer's lead product design. Other than small panel for smartphone, we also have been developing a 0.11 μ m technology specifically for tablet applications.

● Micro-electromechanical Systems (MEMS) Technology

In 2012, TSMC's modular MEMS technology for accelerometer was released and supported the partner customer production ramping. A microphone project for high-resolution noise cancellation applications was executed.

● Flash/Embedded Flash Technology

In 2012, TSMC achieved several milestones in embedded flash technologies at 65/55nm node. The split-gate cell at the 65nm node was qualified for automotive process and is currently in production. For other NOR-type cells, a customer is shipping several prototypes for sampling. For hybrid cells, products for 100k chip card application are in sampling.

At the 40nm node, TSMC has engaged with leading IDMs to develop nitride film storage flash cell and NOR type cell for both automotive and consumer applications.

5.2.3 Technology Platform

TSMC equips modern IC designers with a comprehensive design infrastructure required to optimize productivity and cycle time. This includes design flow for electronic design automation (EDA), silicon-proven building blocks such as libraries and IPs, simulation and verification design kits such as process design kit (PDK) and tech-files. All these are built on top of the technology foundation, and each technology needs its own design infrastructure to be usable for designers. This is the concept of a technology platform.

TSMC's technology platforms reflect the culmination of years of work by TSMC and its alliance partners. The Company has added additional deliverables to its Open Innovation Platform® initiative to further enhance its technology platforms every year since OIP was launched in 2008.

In October 2012, TSMC announced full delivery of 20nm design ecosystem through OIP collaboration. TSMC's 20nm design ecosystem is ready with foundation design collaterals such as DRC, LVS, and PDKs; foundation IPs, including standard-cell libraries, standard I/O, e-Fuse and memory compilers; and standard interface IPs such as USB, PCI, and DDR/LPDDR. Customers can conveniently download these materials at TSMC Online. In addition, new design enablement of EDA tools is updated regularly to satisfy 20nm technology requirements.

TSMC addressed the most critical design challenges through two technology-specific Reference Flows in 2012: 20nm Reference Flow and CoWoS™ Reference Flow. Through these two new reference flows, customers gain access to needed solutions in order to design in TSMC 20nm technology and CoWoS™ technology.

In October 2012, TSMC also announced the foundry segment's 20nm Custom Design Reference Flow, and the fourth revision of the Radio Frequency Reference Design Kit (RF RDK), providing needed design enablement for custom design and RF design.

To ensure timely enhancement of OIP Ecosystem partners' tool compliance with new process requirements, TSMC works with EDA partners to proactively certify EDA tool readiness and publish a report on TSMC online.

Starting from 20nm, the coverage of EDA certification further expanded from DRC, LVS, RC extraction, placement and routing, to static timing analysis, electro-migration, IR drop and custom design.

In order to lower the barrier of technology adoption for customers, TSMC introduced the Integrated Sign-Off Flow (ISF) in 65nm/55nm in 2009, announced 40nm ISF in 2011 and 28nm in 2012. ISF is a production-proven design flow based on TSMC's expertise accumulated over the years. ISF started to bear fruit in 2010, and enabled a large number of first-time customers to leapfrog from 0.13 μ m node to 65nm/55nm node. The introduction of 40nm ISF has further helped customers seize more business opportunities to jumpstart their product solutions, with examples of successful tape-outs for mobile processor application and 3G/4G communication from China in 2011. The newly revealed 28nm ISF in 2012 helped customers seize opportunities in mobile communication with designs in 28nm node.

The Soft-IP Alliance Program aims to improve soft-IP readiness for advanced technology nodes and to drive earlier time-to-market. Soft-IP has historically been process technology independent and therefore not optimized for power, performance, and area considerations. Given the ever-increasing need of first-time silicon success and early time-to-market for highly integrated circuits, such as System-on-Chip (SoC), close technical collaboration between the foundry and the IP provider is imperative to emphasize this critical trade-off.

In 2011, TSMC set up a dedicated quality management system to drive for highest quality assurance for soft-IP continuing the successful story of excellent quality records as seen in hard-IP. Customers can access soft-IP9000 assessment status reports of soft-IPs through TSMC Online. In 2012, the new soft-IP Handoff Package (the soft-IP Kit 2.0) is ready for soft-IP Partners. Soft-IP Kit 2.0 provides an enhanced set of checks that covers such additional design checks as early physical implementation aspects (e.g., area, timing, and congestion) and advanced formal lint checks.

5.2.4 Design Enablement

Customers can design directly using TSMC technologies through the Company's internal design team as well as via alliance partners. TSMC's technology platform provides a solid foundation for design enablement.

Tech File and PDK

Because of TSMC's broader, earlier, and deeper collaboration with customers through the OIP initiative, customers gain greater benefit from TSMC tech-files and process design kit (PDK). The benefits are evidenced by a significant increase to more than 100,000 downloads in 2012, from 50,000 downloads in 2011. TSMC also increased resources to meet the high demand on PDK for specialty technologies.

Library and IP

TSMC and its alliance partners offer TSMC's customers a rich portfolio of libraries and IPs. These reusable building blocks are essential for many design projects. In 2012, over 60% of new tape-outs at TSMC adopted one or more libraries or IPs from TSMC and/or its IP partners. To support the high demand, TSMC also invested resources to expand its library and silicon IP portfolio. The total number of library or IP content in the portfolio, including soft IPs, increased to 5,400 in 2012, compared with 3,740 in 2011.

Design Methodology and Flow

TSMC announced in October 2012 the full delivery of 20nm support within Open Innovation Platform® (OIP) design infrastructure.

TSMC's 20nm design ecosystem is ready with foundation design collaterals such as DRC, LVS, and PDKs; foundation IPs, including standard-cell libraries, standard I/O, e-Fuse & memory compilers; and standard interface IPs such as USB, PCI, and DDR/LPDDR. Customers can download these files at TSMC Online. Collaboration with the EDA community for 20nm has been very thorough in order to achieve tool consistency for improved design results.

20nm Reference Flow features new design solutions/capabilities in place-and-route, RC extraction, DRC, timing analysis, electro migration and IR-drop to enable 20nm designs in double patterning and with characteristics that closely match silicon behavior.

CoWoS™ Reference Flow was announced in October 2012. The emerging 3D integration and process technologies allow the designs with multi-technology support. CoWoS™ Reference Flow enables heterogeneous integration across multiple technologies and memory integration through Wide-IO. In order to satisfy the demands of emerging systems for scaling, performance and functionality, the CoWoS™ Reference Flow provides a complete analysis suite for power integrity, thermal analysis, simultaneously switching noise and innovative DFT and place-and-route solution. With cooperating TSMC ecosystem partners, CoWoS™ design methodology provides the most cost-effective solution for the TSMC recommended design environment. The CoWoS™ design platform can take all benefits of advanced nodes and mature technologies in a very flexible way to achieve target design requirements.

20nm Custom Design Reference Flow enables double patterning capability. It provides solutions to process requirements that are significant in 20nm, including a direct link with simulators for the verification of voltage-dependent DRC rules, an integrated layout-dependent-effect solutions and handling of high-K metal-gate edge effect.

The updated RF RDK provides a solution to address common challenges that RF designers encounter. RF RDK 4.0 offers flexible five-terminal MOS device and accurate noise model for slow wave transmission line. RDK4.0 also offers comprehensive electro-magnetic work flow for radio-frequency passive device synthesis through integrated-passive-device, 60GHz and scalable VCO reference example to assist customers in inductor design.

5.2.5 Intellectual Property

A strong portfolio of intellectual property rights strengthens TSMC's technology leadership and protects our advanced and leading edge technologies. In 2012, TSMC received a record breaking 647 U.S. patents, as well as 300+ issued patents in Taiwan and the PRC, and other patents issued in various other countries. In 2012, TSMC achieved a patent milestone: breaking into the "Top 50" U.S. patent grants in 2012. TSMC's patent portfolio is now approximately 20,000 patents worldwide (includes patent applications in queue). We continue to implement a unified strategic plan for TSMC's intellectual capital management. Strategic considerations and close alignment with the business objectives drive the timely creation, management and use of our intellectual property.

At TSMC, we have built a process to extract value from our intellectual property by aligning our intellectual property strategy with our R&D, business objectives, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities.

We have worked continuously to improve the quality of our intellectual property portfolio and to reduce the costs of maintaining it. We plan to continue investing in our intellectual property portfolio and intellectual property management system to ensure that we protect our technology leadership and receive maximum business value from our intellectual property rights.

5.2.6 TSMC University Shuttle Program

The TSMC University Shuttle Program was established to handle MPW (Multi-Project Wafer) access requests by qualified professors at leading research universities worldwide. To participating professors, TSMC University Shuttle Program provides annual pre-approved access to quality technologies, including 65nm, 40nm process nodes for analog/mixed-signal circuits and RF design, and 0.11 μ m/0.18 μ m process nodes for micro-electromechanical system designs. For very advanced logic design and SRAM researches, the 28nm process node is provided to special university projects. To TSMC, the key performance indices are the 3Rs: Recruiting, Research results transfer from universities to TSMC, and Recognition.

Participations in the TSMC University Shuttle Program include the active participation of major university research groups: in the U.S., M.I.T., Stanford University, UC Berkeley, Harvard University, and UCLA; in Taiwan, National Taiwan University, National Chiao-Tung University, and National Tsing-Hua University; in China, Tsing Hua University in Beijing, and Hong Kong University of Science and Technology, and in Singapore, Nanyang Technological University.

The TSMC University Shuttle Program serves as an effective bridge to link motivated professors and graduate students in leading research universities worldwide with enthusiastic directors and managers at TSMC to contribute to newer level of excellence in advancing technologies and in nurturing new generations of talent in the semiconductor field.

TSMC's University Shuttle Program has been very effective and is praised by professors around the world. They have recognized that this Program allows their graduate students to implement exciting designs ranging from low-power memories, analog-to-digital converters and digital designs to advanced radio-frequency and mixed-signal bio-medical systems. This is a truly "win-win" collaboration. In 2012, TSMC received specific letters of appreciation from professors at M.I.T., Stanford University, UC Berkeley, Harvard University, UCLA, National Taiwan University and National Chiao-Tung University.

5.2.7 Future R&D Plans

In light of the significant accomplishments of TSMC's advanced technologies in 2012, the Company plans to continue to grow its R&D investments. The Company plans to reinforce its exploratory development work on new transistors and technologies, such as 3D structures, strained-layer CMOS, high mobility materials and novel 3D IC devices. These studies of the fundamental physics of nanometer CMOS transistors are core aspects of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to ensure our continued industry leadership at the 28nm and 20nm nodes and to extend our leadership to the 10nm and 7nm nodes. One of TSMC's goals is to extend Moore's Law through both innovative in-house work and by collaborating with industry leaders and academia. We seek to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC intends to continue working closely with international consortia and lithography equipment suppliers to ensure the timely development of 193nm high-NA scanner technology, EUV lithography, and massively parallel e-beam direct-write technologies. These technologies are increasingly important to TSMC's process development efforts at the 10nm, 7nm, and smaller nodes.

TSMC continues to work with mask writing and inspection equipment suppliers to develop viable mask making technology to help ensure that the Company maintains its leadership position in mask quality & cycle time and continues to meet aggressive R&D, prototyping and production requirements.

With a highly competent and dedicated R&D team and its unwavering commitment to innovation, TSMC is confident of its ability to deliver the best and most cost-effective SoC technologies for its customers, thereby supporting the Company's business growth and profitability.

TSMC R&D Future Major Project Summary

Project Name	Description	Risk Production (Estimated Target Schedule)
16nm logic platform technology and applications	Next-generation technology for both digital and analog products	2013
10nm logic platform technology and applications	Exploratory technology for both digital and analog products	2015
3D IC	Cost-effective solution with better form factor and performance for SIP	2013 - 2014
Next-generation lithography	EUV and multiple e-beam to extend Moore's Law	2014 - 2016
Long-term research	Special SoC technology (including new NVM, MEMS, RF, analog) and 10nm transistors	2013 - 2015

The above plans account for roughly 70% of the total R&D budget in 2013, while total R&D budget is currently estimated to be around 8% of 2013 revenue.

5.3 Manufacturing Excellence

5.3.1 GIGAFAB™ Facilities

TSMC's 12-inch fabs are a key part of its manufacturing strategy.

TSMC currently operates three 12-inch GIGAFAB™ fabrication facilities – Fab 12, Fab 14, and Fab 15 – whose combined capacity reached 3,936,000 12-inch wafers in 2012. Production within these three facilities supports 0.13μm, 90nm, 65nm, 40nm, 28nm, and 20nm process technologies, and their sub-nodes. Part of the capacity is reserved for research and development work and currently supports 16nm, 10nm and beyond technology development. TSMC has developed a centralized fab manufacturing management for the customers' benefit of consistent quality and reliability performance, greater flexibility of demand fluctuations, faster yield learning and time-to-volume, and minimized costly product re-qualification. It enables Fab 15 to fast ramp 28nm capacity from zero to 50,000 wafers output per month in eight months to satisfy customers' demand.

5.3.2 Engineering Performance Optimization

Highly sophisticated information technology (IT) solutions, such as advanced equipment control, fault detection and diagnosis, engineering big data mining, and centralized operation platforms, are implemented to optimize TSMC equipment, process and yield performance. They also improve production efficiency, effectiveness, and engineering capability via information integration, workflow optimization and automation.

Advanced analytical methods identify critical equipment and process parameters that are linked to device performance. Methodologies such as virtual metrology, yield dissection and management integrate Advanced Process Control (APC), Fault Detection Classification (FDC), Statistical Process Control (SPC), and Circuit Probe data in order to optimize equipment performance to match device performance.

Accurate modeling and control at each process stage drives intelligent module loop control. The process control hierarchy dispatched via sophisticated computer-integrated manufacturing systems enables optimization from equipment to end product, which achieves precision and lean operation in a high product mix semiconductor manufacturing environment.

5.3.3 Precision and Lean Operations

TSMC's unique manufacturing infrastructure is tailored for a high product mix foundry environment. Following its commitment to manufacturing excellence, TSMC has equipped a sophisticated scheduling and dispatching system, implemented industry-leading automated materials handling systems, and employed Lean Manufacturing approaches to provide customers with on-time-delivery and best-in-class cycle time. Real-time equipment performance and productivity monitoring, analysis, diagnosis and control minimize production interruption and maximize cost effectiveness.

5.3.4 450mm Wafer Manufacturing Transition

TSMC joined the Global 450mm Consortium (G450C) located in the College of Nanoscale Science and Engineering (CNSE) of New York University at Albany, New York. The consortium includes five IC makers and CNSE (which represents New York State and provides the clean room facility), as well as key 450mm tool suppliers as associate members.

Currently, TSMC has 16 experienced employees working in the consortium. TSMC has assumed the Operation GM position in the consortium and commits to lead the industry for a cost-effective 450mm transition. The clean room of G450C in Albany has been ready for tool installation since Q1 2013. The majority of the tools will be installed in 2013.

Besides 450mm tool readiness, TSMC is also developing novel 450mm operation to bring the maximum value of semiconductor wafer fabrication to customers, including advanced quality and the most competitive cycle time in advanced technology. 450mm will be a new era of semiconductor manufacturing with new manufacturing capability advanced from today's leading edge technology.

5.3.5 Raw Materials and Supply Chain Risk Management

In 2012, TSMC continued Supply Chain Risk Management meetings periodically to integrate Company resources from materials management, fab operations, risk management and quality management. TSMC worked with its suppliers to enhance the performance of quality, delivery, risk management, and to support green procurement, environmental protection and safety.

Raw Materials Supply

Major Materials	Major Suppliers	Market Status	Procurement Strategy
Raw Wafers	F.S.T. MEMC S.E.H. Siltronic SUMCO	These five suppliers together provide over 90% of the world's wafer supply. Each supplier has multiple manufacturing sites in order to meet customer demand, including plants in North America, Asia, and Europe.	<ul style="list-style-type: none"> TSMC's suppliers of silicon wafers are required to pass stringent quality certification procedures. TSMC procures wafers from multiple sources to ensure adequate supplies for volume manufacturing and to appropriately manage supply risk. TSMC maintains competitive price and service agreements with its wafer suppliers, and, when necessary, enters into strategic and collaborative agreements with key suppliers. TSMC regularly reviews the quality, delivery, cost and service performance of its wafer suppliers. The results of these reviews are incorporated into TSMC's subsequent purchasing decisions. A periodic audit of each wafer supplier's quality assurance systems ensures that TSMC can maintain the highest quality in its own products.
Chemicals	Air Products ATMI BASF Dow KANTO-PPC MGC	These six companies are the major suppliers for bulk and specialty chemicals.	<ul style="list-style-type: none"> Most suppliers have relocated many of their operations closer to TSMC's major manufacturing facilities, thereby significantly improving procurement logistics. The suppliers' products are regularly reviewed to ensure that TSMC's specifications are met and product quality is satisfactory.
Litho Materials	AZ Dow JSR Nissan Shin-Etsu Chemical Sumitomo T.O.K.	These seven companies are the major suppliers for worldwide litho materials	<ul style="list-style-type: none"> TSMC works closely with its suppliers to develop materials able to meet application and cost requirements. TSMC and suppliers periodically conducts improvement programs of their quality, delivery, sustainability and green policy, to ensure continuous progress of TSMC's supply chain.
Gases	Air Liquide Air Products Linde Taiyo Nippon Sanso	These four companies are the major suppliers of specialty gases.	<ul style="list-style-type: none"> The majority of the four suppliers are located in different geographic locations, minimizing supply risk to TSMC. TSMC conducts periodic audits of the suppliers' quality assurance systems to ensure that they meet TSMC's standards.
Slurry, Pad, Disk	Asahi Glass Cabot Microelectronics DA Nano Dow Chemical Fujifilm Planar Solutions Fujimi Hitachi Chemical Kinik 3M	These nine companies are the major suppliers for CMP materials.	<ul style="list-style-type: none"> TSMC works closely with its suppliers to develop materials able to meet application and cost requirements. TSMC and suppliers periodically conducts improvement programs of their quality, delivery, sustainability and green policy, to ensure continuous progress of TSMC's supply chain.

Suppliers Accounted for at Least 10% of Annual Consolidated Net Procurement

Unit: NT\$ thousands

Supplier	2012			2011		
	Procurement Amount	As % of 2012 Total Net Procurement	Relation to TSMC	Procurement Amount	As % of 2011 Total Net Procurement	Relation to TSMC
Company A	6,708,942	16%	None	5,549,444	22%	None
Company B	5,846,449	14%	None	3,035,441	12%	None
VIS	4,475,674	11%	Investee accounted for using equity method	5,597,895	22%	Investee accounted for using equity method
SSMC	3,638,633	9%	Investee accounted for using equity method	3,949,176	16%	Investee accounted for using equity method
Others	20,710,694	50%		6,775,433	28%	
Total Net Procurement	41,380,392	100%		24,907,389	100%	

5.3.6 Quality and Reliability

A characteristic of TSMC's industry reputation is its commitment to providing customers with the best quality wafers and service for their products. Quality and Reliability (Q&R) services aim to achieve "quality on demand" to fulfill customers' needs regarding time-to-market, reliable quality, and market competition over a broad range of products.

Q&R technical services assist customers in the technology development and product design stage to design-in their product reliability requirements. Since 2008, Q&R has worked with R&D to successfully establish and implement new qualification methodology for High-k/Metal Gate (HKMG). Q&R also works with design services on embedded memory, high voltage, e-Fuse and MEMS IP developments to expand TSMC's design portfolio. Since 2009, Q&R has worked with R&D and the design service team to improve the quality of design kits through integrated R&D and design quality platform. In 2012, Q&R continued to work with R&D and the design team to develop DRM infrastructure with iEDA layout platform. Q&R also deployed an SRAM cell review system to improve bit cell change quality of third parties and customers. Q&R has been collaborating with SEMI to establish an IC Quality Committee since May in order to enhance product quality of the semiconductor supply chain. For backend technology development, Q&R worked with R&D, BTSD (Backend Technology and Service Division) and Product Engineering to complete the CoWoS™ technology development and production transfer. After establishing Power Cycling capability and methodology in 2011, Q&R will further extend backend characterization by adding system-level temperature cycling, bending, drop and vibration tests in 2013.

Q&R has deployed systems to ensure robust quality in managing production and in design services, including third-party IP management, to meet the business requirements of customers. Q&R also implemented innovative statistical matching methodologies to enhance manufacturing quality, including matching of facility, metrology and process tools, wafer acceptance test (WAT) data and reliability performance. In 2011, Q&R tightened the post-fab outgoing visual inspection criteria for wafer quality improvement to AQL 0.4% from AQL 0.65%.

To sustain production quality and to minimize risk to customers when deviations occur, manufacturing quality monitoring and event management span all critical stages – from raw material supply, mask making, and real-time in-process monitoring, to bumping, wafer sort and reliability performance. Advanced failure and materials analysis techniques are also developed and effectively deployed in process development, customer new product development and product manufacturing. In addition to adapting analytical techniques to aid in the release and monitoring of advanced Fab tools and processes for advanced technology nodes, state-of-the-art electron microscopy,

chemical analysis and fault isolation equipment were added at a record pace in 2012 to support development activities of the 20nm and 16nm technology nodes.

In compliance with the electronic industry's lead-free and green IC package policy, Q&R qualified and released lead-free bumping to satisfy customer demands, and made lead-free bump package possible for 0.13μm, 45nm, 40nm and 28nm technology products by collaborating with the major outsource assembly & testing subcontractors (OSAT). This enabled TSMC customers to introduce and ramp lead-free products with excellent assembly quality. In 2012, TSMC Q&R ramped wafer-level Chip Scale Package (CSP) to 20K per month and lead-free to 40K per month without major quality issues. For mainstream technologies, Q&R qualified ultra, extreme low leakage and high endurance embedded Flash IP, IPD (Integrated Passive Device), hybrid of Copper, Copper-Aluminum technology with customers. Q&R continues to build reliability testing and monitoring to ensure excellent manufacturing quality of automotive, high-voltage products, CMOS image sensors and embedded-Flash memory products.

TSMC Q&R is also responsible for leading the Company towards the ultimate goal of zero-defect production through the use of continuous improvement programs. Periodic customer feedback indicates that products shipped from TSMC have consistently met or exceeded their field quality and reliability requirements. In 2012, a third-party audit verified the effectiveness of the TSMC quality management system (including R&D labs) in compliance with ISO/TS 16949:2009 and IECQ QC 080000 certificates requirements.

5.4 Customer Trust

5.4.1 Customers

TSMC's worldwide customers have diverse product specialties and excellent performance records in various segments of the semiconductor industry. Fabless customers include: Advanced Micro Devices, Inc., Altera Corporation, Broadcom Corporation, Marvell Semiconductor Inc., MediaTek Inc., NVIDIA Corporation, OmniVision Technologies and Qualcomm Inc. IDM customers include: Analog Devices Inc., STMicroelectronics and Texas Instruments Inc. etc.

Customer Service

TSMC believes that providing superior customer service is critical to enhancing customer satisfaction and loyalty, which is the path to retaining existing customers, attracting new customers, and strengthening customer relationships. With a dedicated customer service team as a main contact window for coordination and facilitation, TSMC strives to provide world-class, high-quality, efficient and professional services in design support, masking, manufacturing, and backend to achieve optimum experience for our customers and, in return, to gain customer's trust and sustain Company profitability.

To facilitate customer interaction and information access on a real-time basis, TSMC's EFOUNDRY® services offer a suite of web-based applications that provide a more active role in design, engineering, and logistics. Designers have 24-hour a day, seven-day-a-week access to critical information and are able to create custom reports through EFOUNDRY® online services. Design Collaboration focuses on content availability and accessibility, with close attention to complete, accurate, and current information at each level of the wafer design life cycle. Engineering Collaboration includes online access to engineering lots, wafer yields, wafer acceptance test (WAT) analysis, and quality reliability data. Logistics Collaboration provides access to data updated three times a day on any given wafer lot's status in order, fabrication, assembly and testing, and shipping.

Customer Satisfaction

To assess customer satisfaction and to ensure that as many as possible of our customers' needs and wants are adequately addressed, TSMC conducts an annual customer satisfaction survey (ACSS) with all active customers, either by web or interview survey, through an independent consultancy.

Complementary with ACSS, quarterly-based business reviews (QBRs) are also performed by the customer service team to survey customers' satisfaction during their visits on technical and business related services offered. Through both surveys and intensive interaction with customers by account team, TSMC is able to maintain close touch with customers for better service and collaboration.

All customer feedback is routinely reviewed by executives and developed into improvement plans to become an integral part of this survey process with a complete closed-loop. TSMC has maintained a focus on customer survey data as one key indicator of corporate performance – not just of past performance, but also as a leading indicator of future performance. TSMC has acted on the belief that satisfaction leads to loyalty, and customer loyalty leads to higher levels of retention and expansion.

Customers Accounted for at Least 10% of Annual Consolidated Net Sales

Unit: NT\$ thousands

Customer	2012			2011		
	Net Sales	As % of 2012 Total Net Sales	Relation to TSMC	Net Sales	As % of 2011 Total Net Sales	Relation to TSMC
Customer A	85,357,353	17%	None	59,203,844	14%	None
Others	420,891,227	83%		367,876,801	86%	
Total Net Sales	506,248,580	100%		427,080,645	100%	

5.4.2 Open Innovation Platform® (OIP) Initiative

Innovation has long been both an exciting and challenging proposition. Competition among semiconductor companies is becoming more active and intense in the face of increasing customer consolidation and the commoditization of technology at more mature, conventional levels. Companies must find ways to continue innovating in order to prosper further. Companies innovating openly from the "outside in" as well as from the "inside out" accelerate innovation through active collaborations with external partners. This active collaboration of TSMC with external partners is known as Open Innovation. TSMC has adopted this path to innovate via the Open Innovation Platform® (OIP) initiative.

The TSMC Open Innovation Platform® (OIP) initiative is a comprehensive design technology infrastructure that encompasses all critical IC implementation areas to reduce design barriers and improve first-time silicon success. OIP promotes the speedy implementation of innovation amongst the semiconductor design community and its ecosystem partners with TSMC's IPs, design implementation and DFM capabilities, process technology and backend services.

A key element of OIP is a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that more efficiently empowers innovation throughout the supply chain and, in turn, drives the creation and sharing of newly-created revenue and profits. TSMC's Active Accuracy Assurance (AAA) initiative is critical to OIP, providing the accuracy and quality required by the ecosystem interfaces and collaborative components.

TSMC's Open Innovation model brings together the innovative thinking of customers and partners under the common goal of shortening design time, minimizing time-to-volume and speeding time-to-market and, ultimately, time-to-revenue:

- The foundry segment's largest, most comprehensive and robust silicon-proven intellectual properties (IPs) and library portfolio;
- Advanced design methodology delivery through reference flows, design for manufacturing (DFM), and process design kits; and
- Comprehensive design ecosystem alliance programs covering market-leading EDA, library, IPs, and design service partners.

TSMC's OIP Alliance consists of 30 electronic design automation (EDA) partners, 41 IP partners, and 26 design service partners. TSMC and its partners proactively work together, and engage much earlier and deeper than before in order to address mounting design challenges at advanced technology nodes. Through this early and intensive collaboration effort, TSMC OIP is able to deliver the needed design infrastructure with timely enhancement of EDA tools, early availability of critical IPs and quality design services when customers need them. This is critical to success for the customers to take full advantage of the process technologies once they reach production-ready maturity.

In October 2012, TSMC hosted OIP Ecosystem Forum at San Jose Convention Center in California, with keynote addresses from the executives of TSMC as well as OIP ecosystem partners. The forum was well attended by both customers and ecosystem partners and demonstrated the value of collaboration through OIP to nurture innovations.

TSMC's OIP Partner Management Portal facilitates communication with our ecosystem partners for efficient business productivity. This portal is designed with an intuitive interface and can be linked directly from TSMC-Online.

5.5 Employees

5.5.1 Human Capital

Human capital is one of the most important assets of TSMC. The Company strives to provide employees with a challenging, enjoyable and rewarding work environment. In 2012, TSMC was named the "Most Admired Company in Taiwan" by *CommonWealth Magazine* for the 16th consecutive year.

At the end of 2012, TSMC had over 37,000 employees worldwide, including 3,614 managers and 15,264 professionals. Female managers comprised 11.4% of all managers, and non-Taiwanese nationals comprised 8.5% of all TSMC managers and professionals. In addition, when consolidating TSMC and all its subsidiaries, we had over 39,000 employees at the end of 2012. The following table summarized TSMC workforce structure at the end of February, 2013:

TSMC Workforce Structure

		12/31/2011	12/31/2012	02/28/2013
Job	Managers	3,374	3,614	3,652
	Professionals	13,111	15,264	15,594
	Assistant Engineer/ Clerical	2,745	3,006	3,084
	Technician	14,439	15,265	15,199
Total		33,669	37,149	37,529
Gender	Male	54.1%	56.2%	56.7%
	Female	45.9%	43.8%	43.3%
Education	Ph.D.	3.5%	3.6%	3.7%
	Master's	32.8%	35.3%	35.7%
	Bachelor's	25.9%	25.6%	25.7%
	Other Higher Education	13.9%	13.0%	12.7%
	High School	23.9%	22.5%	22.2%
Average Age (years)		33.0	33.3	33.4
Average Years of Service (years)		6.2	6.4	6.4

5.5.2 Recruitment

TSMC advocates equal opportunity employment, and its practices center on the principles of open-and-fair recruitment. We consider the candidate according to his/her qualification as related to the requirement of each position, rather than race, gender, age, religion, nationality, or political affiliation.

Although facing a stagnated global economy, TSMC's continuous growth requires constant talent sourcing and recruitment activities to support its business. We recruited over 3,600 managers and professionals, and 2,000 assistants and technicians in 2012.

In order to cultivate a young talent pipeline for recruitment around the world, TSMC deploys a number of recruiting activities and university programs, including Joint Development Programs, University Shuttle Program, Summer Internship; Job Fairs in Taiwan, U.S., Singapore and India, Fresh Graduate Career Symposium, and Outstanding Student Research Award. These programs also advance novel or innovative academic semiconductor research.

5.5.3 People Development

TSMC has committed to cultivating a continuous and diversified learning environment. Under this mission, we established the Procedure of Employee Training and Education to ensure the Company's and individuals' development objectives can be achieved through internal and external training resources.

The Company provides employees with a wide range of on-site general, professional and management training programs. In addition to external experts engaged as trainers, hundreds of TSMC employees are trained as qualified instructors for delivering valuable know-how in internal training courses. During 2012, TSMC conducted 1,377 internal training sessions, for a company-wide total of over 780,000 training hours and a total of 520,000 attendees participating. Employees on average attended 21 hours of training. The total training expenses were almost NT\$60 million. TSMC's training programs include:

- **New Employee Training:** includes new employee basic training and job orientation. Furthermore, newcomers' manager and our well-established Buddy System are actively engaged in the assimilation process.
- **General Training:** refers to training required by government regulations and/or Company policies. Such training includes subjects of industry-specific safety, workplace health and safety, quality, fab emergency response, languages, and personal effectiveness training.
- **Professional/Functional Training:** provides technical and professional training required by various functions within the Company. We offer training courses on equipment engineering, process engineering, accounting, and information technology, and so forth.
- **Management Training:** programs tailored to the needs of managers at all levels, including New, Experienced, and Senior Manager programs, as well as other elective courses.
- **Direct Labor (DL) Training:** enables production line employees to acquire the knowledge, skills and attitudes they need to perform their job well and to pass the certification for operating equipment. Training includes DL Skill Training, Technician "Train-the-Trainer" Training, and Manufacturing Leader Training.

Based on individual job nature, work performance and career development track, a tailor-made Individual Development Plan (IDP) is established for each employee. Meanwhile, our employees are provided with a comprehensive network of learning resources, including on-the-job training, coaching, mentoring, job rotation, on-site training and e-learning. They are also subsidized when taking external short-term courses, credit courses and degrees.

5.5.4 Employee Satisfaction

TSMC is committed to providing above-industry-average quality jobs to its employees, and it is dedicated to foster a dynamic and fun work environment. The Company encourages employees to maintain a healthy and well-balanced life, apart from their time spent working.

TSMC's commitment in employee caring and its unceasing efforts as an advocator of employees' work-life balance has earned it the prestigious first place as the "Happiest Corporation" of the Top 10 Happy Corporations, released by China Credit Information Service (CCIS), under its survey released in the second half of 2012.

To enrich employees' work experience, the Company continuously implements programs to enhance employee caring, benefits, rewards and communication. The various initiatives include the following:

Employee Benefit Programs

- **Diverse employee welfare programs:** employees can enjoy 70 hobby clubs, 45 speeches covering diverse topics (in 2012), Sports Day, Family Day and so on. In addition, holiday bonuses, marriage bonuses, condolence allowances and emergency subsidies are also available to cater for employees' needs.
- **Convenient on-site services:** cafeteria, dry-cleaning, convenience store, travel, banking, haircutting service, housing, and commuting assistance are accessible for employees in the fabs, ensuring the highest convenience of daily-life necessities for employees at work.
- **Comprehensive health enhancement programs:** physical care and psychological consultation services are available to employees to ensure their well-being. Five free counseling sessions are offered to TSMC employees on an annual basis, with extension available depending on the individual's needs. Additional health enhancement programs provided by TSMC include weight control, medical check-up, smoking cessation, exercise camp, massage service, sleep assistance, abdominal and neck x-ray, female care, blood donation, liver disease prevention, monthly seminar, etc.
- **Premium Sports Center:** with a variety of workout facilities to all employees and their families, as well as exercise sessions conducted by professional instructors available for employees' choices to promote a healthier lifestyle.
- **Flexible Preschool Service:** the service, operated as per employees' working time to meet their need for childcare, is available in Hsinchu and Tainan. In 2012, TSMC's preschool was recognized as the "Premium Corporate Facility" by Taiwan's Council of Labor Affairs.

Employee Recognition

TSMC sponsors various award programs to recognize employees' outstanding achievement, both as a team or on the individual level. With these award programs, TSMC aims to encourage employees' sustainable development that in turn adds to the Company's competitive advantage.

The various award programs sponsored by TSMC include:

- **TSMC Medal of Honor,** presented exclusively by Chairman, recognizes those who contribute to the Company's business performance significantly.
- **TSMC Academy** recognizes outstanding TSMC scientists and engineers whose individual technical capabilities make significant contributions to the Company.
- **Outstanding Engineer Award** for each fab and **Total Quality Excellence Conference Award** recognize employees' continuous efforts in creating value for the Company.
- **Service Award** represents TSMC's appreciation toward senior employees' dedication and commitment to the Company.
- **Excellent Instructor Award** praises the outstanding performance and contribution of the Company's internal instructors in training courses.

In 2012, TSMC employees continued to be recognized through a host of prestigious external awards, including Top 10 National Outstanding Managers Award, Outstanding Engineer Award, Outstanding Young Engineer Award, as well as National Industrial Innovation Award.

Employee Communication

TSMC values two-way communication and is committed to keeping the communication channels between the management level and their subordinates, as well as among peers, open and transparent. Our continuous efforts lie in reinforcing mutual and timely employee communication, based on multiple channels and platforms, which in turn fosters harmonious labor relations and creates a win-win situation for the Company and the employees.

A host of channels, including both face-to-face and virtual, are leveraged to maintain the unobstructed flow of information between the management level of the Company and the employees, including:

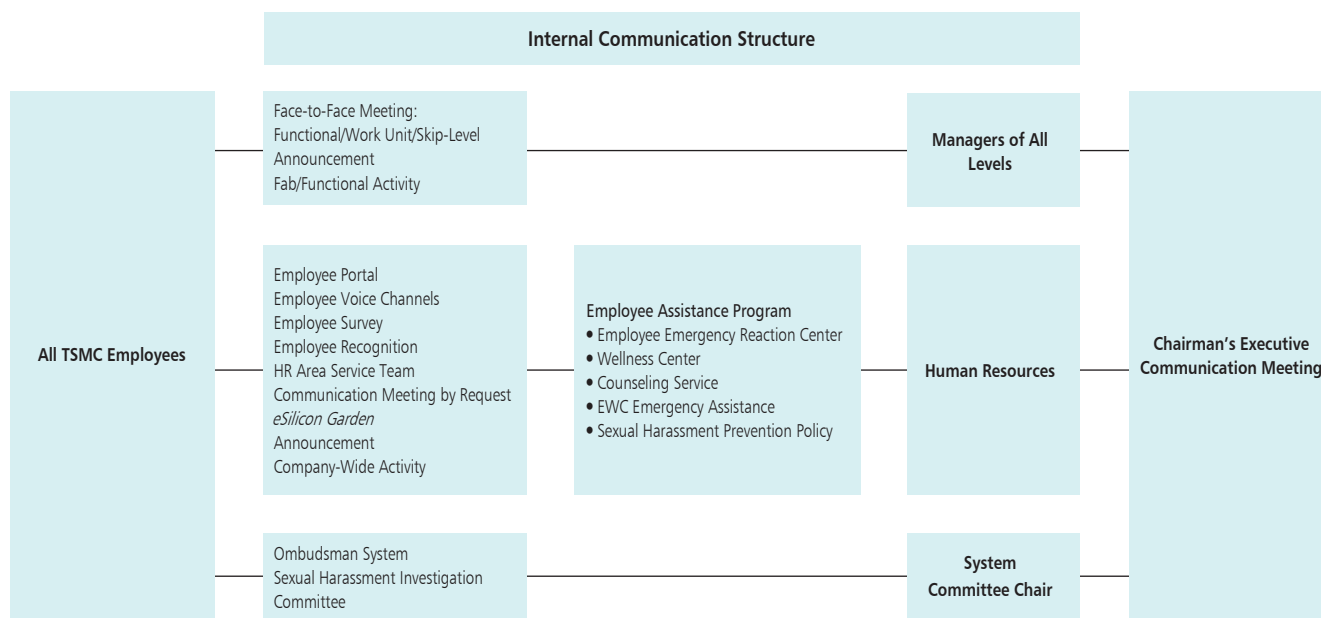
- Regular communication meetings held for the various levels of managers and employees.
- Periodic employee satisfaction surveys and follow-up actions based on the survey findings.
- Enhanced corporate employee portal (myTSMC 2.0):
 - Corporate messages, executive interviews, employee activities and so on are posted on the intranet for employees' timely reference.
 - Important talks from Chairman are webcasted via the intranet to reach employees worldwide.
- *eSilicon Garden*: The website hosting TSMC's internal publication, available in both Chinese and English, is updated on a bi-weekly basis with its content ranging from work to run.

To ensure that employees' opinions and voices are heard, and their issues are addressed and solved, impartial and smooth voice submission mechanisms, including quarterly labor-management communication meetings, are in place to provide timely support.

- Complaints regarding major management, financial and auditing issues are directed to the following channels, which handle the complaints with high level of confidentiality:
 - The independent Audit Committee; and
 - Ombudsman system led by an appointed Vice President.
- The Suggestion Box provides a channel for employees to express their opinions regarding their work and the overall work environment.
- Employee care teams in each fab take care of the issues related to employees' work and personal life.

The Company also sets and promotes policies and measures to ensure gender equity in accordance with employment laws and sexual harassment prevention policies to foster a fair work environment for employees of both genders.

All in all, the comprehensive communication channels provided by TSMC can be showcased by the following chart:



5.5.5 Retention

From the employee's initial adaptation to professional and career development, TSMC works proactively to retain outstanding employees through creating an innovative, challenging, and fun environment. All these efforts contributed to a healthy turnover rate of 5.7% for 2012.

5.5.6 Compensation

TSMC provides a diversified and competitive compensation program that is competitive externally, fair internally, and adapted locally. TSMC upholds the philosophy of sharing wealth with employees in order to attract, retain, develop, motivate and reward talented employees. With excellent operating performance, employment at TSMC entitles employees to a comprehensive compensation and benefits program above the industry average.

TSMC's compensation program includes a monthly salary, an employee cash bonus based on quarterly business results, and employee profit sharing when the Company distributes its profit each year.

The purpose of the employee cash bonus and profit sharing programs is to reward employee contributions appropriately, to encourage employees to work consistently toward ensuring the success of TSMC, and to link employees' interests with those of TSMC's shareholders. The Company determines the amount of the cash bonus and profit sharing based on operating results and industry practice in the Republic of China. The amount and form of the employee cash bonus and profit sharing are determined by the Board of Directors based on the Compensation Committee's recommendation, and the employee profit sharing is subject to shareholders' approval at the Annual Shareholders' Meeting. Individual awards are based on each employee's job responsibility, contribution and performance.

In addition to providing employees of TSMC's overseas subsidiaries with a locally competitive base salary, the Company grants short-term and long-term bonuses as a part of total compensation. The performance bonus is a short-term incentive and is granted in line with local regulations, market practices, and the overall operating performance of each subsidiary. The long-term incentive bonus is awarded based on TSMC's financial performance and is vested over the course of several years in order to encourage long-term employee commitment and development within the Company.

5.5.7 Retirement Policy

TSMC's retirement policy is set according to the Labor Standards Act and Labor Pension Act of the Republic of China. With the Company's sound financial system, TSMC ensures employees a solid pension contribution and payments, which encourages employees to set long-term career plans and raises their commitment to TSMC.

5.6 Material Contracts

Shareholders Agreement

Term of Agreement:

Effective as of 03/30/1999 and may be terminated as provided in the agreement

Contracting Parties:

Koninklijke Philips Electronics N.V. (Philips) and EDB Investments Pte Ltd. (EDBI)

(In September 2006, Philips assigned its rights and obligations under this agreement to Philips Semiconductors International B.V. which has now been renamed NXP B.V. In November 2006, NXP B.V. and TSMC purchased all SSMC shares owned by EDBI; EDBI is no longer a contracting party to this agreement.)

Summary:

TSMC, Philips and EDBI had formed a Singapore joint venture "Systems on Silicon Manufacturing Company Pte Ltd." (SSMC) for providing semiconductor foundry services. Philips Semiconductor (now NXP B.V.) and TSMC are committed to purchasing a certain percentage of SSMC's capacity.

Technology Cooperation Agreement

Term of Agreement:

03/30/1999 - 03/29/2004, automatically renewable for successive five-year terms until and unless either party gives written notice to terminate one year before the end of then existing term

Contracting Party:

Systems on Silicon Manufacturing Company Pte Ltd. (SSMC)

Summary:

TSMC agreed to transfer certain process technologies to SSMC, and SSMC agreed to pay TSMC a certain percentage of the net selling price of SSMC products.

Patent License Agreement

Term of Agreement:

12/20/2007 - 12/31/2017

Contracting Party:

A multinational company

Summary:

The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting company.

Manufacturing, License, and Technology Transfer Agreement

Term of Agreement:

04/01/2004 - 03/31/2006, automatically renewable for successive one-year terms until and unless both parties decide otherwise by mutual consent in writing

Contracting Party:

Vanguard International Semiconductor Corporation (VIS)

Summary:

VIS reserves certain capacity to manufacture TSMC products on mutually agreed terms. TSMC may also transfer certain technologies to VIS, for which it will in return receive royalties from VIS.

Patent License Agreement

Term of Agreement:

11/01/2002 - 10/31/2012

Contracting Party:

A multinational company

Summary:

The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting party.

Amended Research and Development Collaboration Agreement

Term of Agreement:

01/01/2009 - 12/31/2009, renewable on annual basis upon mutual agreement

Contracting Party:

NXP B.V.

Summary:

The parties entered into research and development collaboration to develop advanced semiconductor technologies.

Investment Agreement & Shareholder Agreement

Term of Investment Agreement:

08/05/2012 - 04/15/2013

Term of Shareholder Agreement:

Effective as of 10/31/2012 and may be terminated as provided in the agreement

Contracting Party:

ASML Holding N.V. (ASML)

Summary:

TSMC joined the Customer Co-Investment Program of ASML Holding N.V. (ASML) and entered into the investment agreement and shareholder agreement. The agreements include an investment of EUR837,815,664 by TSMC Global to acquire a non-voting 5% in ASML's equity with a lock-up period of 2.5 years.

Research and Development Funding Agreement

Term of Agreement:

10/31/2012 - 12/31/2017

Contracting Party:

ASML Holding N.V. (ASML)

Summary:

TSMC will provide EUR277 million to ASML's research and development programs from 2013 to 2017.

Note: TSMC is not currently party to any other material contract, other than contracts entered into in the ordinary course of our business. The Company's "Significant Commitments and Contingencies" are disclosed in Annual Report (II), Financial Information, page 68-69.