Unceasing pursuit of innovation in strategy, sales, management, technology, and manufacturing, is the wellspring of our growth.
5. Operational Highlights

5.1 Business Activities

5.1.1 Business Scope

As the founder and a leader of the dedicated IC foundry segment, TSMC has built its reputation by offering advanced and “More-than-Moore” wafer production processes and unparalleled manufacturing efficiency. TSMC strives to provide the best overall value to customers, and the success of TSMC’s business is manifested in the success of its customers.

TSMC provides a full range of integrated IC foundry services that fulfill the increasing variety of customer needs. In the process, it has experienced strong growth by building partnerships with customers. IC suppliers from around the world trust TSMC with their manufacturing needs, thanks to its unique integration of cutting-edge process technologies, pioneering design services, manufacturing productivity and product quality.

In May 2009, TSMC established the New Businesses organization to explore non-foundry related business opportunities. During 2010 and early 2011, the New Businesses organization consists of two business divisions responsible for solid state lighting and solar business activities.

5.1.2 Customer Applications

Over the past 23 years, more than 600 customers worldwide have relied on TSMC to manufacture chips that are used across the entire spectrum of electronic applications, including computers and peripherals, information appliances, wired and wireless communications systems, automotive and industrial equipment, consumer electronics such as DVDs, digital TVs, game consoles, digital still cameras (DSCs), and many other applications.

The rapid evolution of end products drives our customers to utilize TSMC’s innovative technologies and services, while at the same time spurring TSMC’s own development of technology. As always, success depends on leading rather than following industry trends.
5.1.3 Unconsolidated Shipments and Gross Sales in 2010 and 2009

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<th>2010</th>
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5.1.4 Production in 2010 and 2009

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</table>

5.2 Technology Leadership

5.2.1 R&D Organization and Investment

TSMC expanded Research and Development in 2010 to further enhance one of its three strategic pillars: Technology Leadership. In 2010 the total R&D budget was 7% of total revenue. This level of R&D investment is equal to or more than that of many leading edge technology companies. Along with the budget increase, the R&D organization increased staffing by over 17%.

TSMC recognizes that the technology challenge required to extend Moore’s Law, the business law behind CMOS scaling, is getting increasingly difficult. Dr. Shang-yi Chiang, TSMC Senior Vice President of R&D brings his rich industry experience to lead the strengthening of the R&D team and to navigate through the technological and competitive challenges ahead.

In 2010, TSMC offered the foundry segment’s first 28nm technology. After intense work on ramping this technology, customers started to experience its benefits of stable and improved yield.

TSMC accelerated the development of advanced transistors, embedded memories, and copper (Cu)/low-K interconnect technologies. During 2010, the R&D organization once again proved its capabilities by offering a first-to-market 28nm high-K/metal gate (HKMG) foundry technology portfolio as well as establishing 20nm path-finding capability.

TSMC also expanded its external R&D partnerships and alliances with world-class research institutions. For example, TSMC is a core partner of IMEC, the respected European R&D consortium. TSMC also has a strategic agreement with IP provider to enable the development of physical IP through the advanced technology nodes. In addition, TSMC strengthened its collaborations with key partners on design-process optimization. TSMC provides funding for nanotechnology researches at major universities worldwide to promote innovation and the advancement of technology.

These research efforts enable the Company continuously to offer its customers the foundry-leading, first-to-market technology and design solutions that contribute to their product success in the complex and challenging market environment.
5.2.2 R&D Accomplishments in 2010

R&D Highlights

- **28nm Technology**
  TSMC continued to lead the foundry segment with the development of the most advanced logic technologies both with conventional as well as HKMG stacks. The high performance (28HP) platform is aimed at high-speed GPU and CPU applications. It also serves as the technology backbone for high-end FPGA and SoC application domains through additional device customization for leakage management. The low-leakage (28LP and 28HPL) technologies are designed to support low-cost mobile applications as well as low-end FPGA requirements.

With the improvement and development momentum, TSMC has continuously demonstrated breakthroughs in both 64Mb SRAM yield and technology reliability for all the 28nm technology family, including 28LP, 28HP and 28HPL. In addition, 28LP has completed the technology qualification in September 2010 and proved to be the first 28nm technology within the semiconductor and foundry industries ready for risk production. HKMG technology qualification is also under way.

In parallel, TSMC provided 28nm shuttle service program and successfully delivered proven and functional test-chips for both conventional SiON/poly and HKMG technologies. More than 10 shuttle services were offered in 2010, and more than 25 customers validated their test-chips and critical IPs with TSMC’s 28nm technologies for various market segments, including GPU/CPU, FPGA and mobile applications.

- **20nm Technology**
  In 2010, TSMC continued to focus on 20nm technology path finding and development. To offer a leading-edge technology for both analog and digital application, the Company adopted the most advanced 193nm immersion and enhanced lithography process for smaller feature size. With the second generation of HKMG, more Si strain, and new device structure, the intrinsic transistor performance continues to ramp following Moore’s Law. Meanwhile, external resistance can be effectively reduced and controlled by a specially designed process technique. The back end-of-line (BEOL) interconnect process features extreme low-K intermetal dielectric materials and copper metallization with the novel low-resistance scheme. The logic transistor and SRAM bit-cell offering, using the 20nm process, will cover high performance and System-on-Chip (SoC) application.

Development of 20nm technology will create superior gate density and chip performance. The cost and complexity of advanced technology will continue to escalate for customers. In 2010, TSMC provided process flow, design kits and intellectual property (IP) to help reduce foundry costs. TSMC’s high-performance 20nm process will enter risk production in the third quarter of 2012, with volume production scheduled for the first quarter of 2013.

- **Lithography**
  To overcome unprecedented low k, for imaging, state-of-the-art optical lithography resolution enhancement techniques, such as source-mask optimization and multiple patterning, have been implemented to achieve 2X the gate density of previous generation. Combined with an optimized etching technique and film stack, a nonlinear photoresist was introduced to achieve a 2.2nm line-width-roughness (LWR) on the switching gates to gain device performance.

The reticle for Test Vehicle 1 of the 20nm node was taped out in mid 2010 with an advanced super binary intensity mask (BIM) blank. The overlay control for inter- and intra-layers reached 6nm, a 25% gain from the previous generation. Moreover, with design rule optimization, the patterning technique of the active layer can be simplified from 3P2E to 2P2E, resulting in significant cost reduction.

Low-single-digit immersion defects for the 28nm node were achieved with track/material co-optimization that evolved from and is better than the previous generation. To deal with various product requirements, customized OPC was used. Low-cost solutions were developed for 0.11μm logics, multi-generation technologies, and special technologies such as eDRAM and CMOS Image Sensor (CIS).

For next generation lithography (NGL) technology development, a multiple e-beam maskless pre-Alpha tool installed in TSMC’s fab has been demonstrating imaging with 110 beams and patterns of the 20nm node using e-beam proximity correction.

In early 2010, the Company announced the acquisition of a full-field extreme-ultraviolet (EUV) scanner from ASML Netherlands B.V. for the development of lithographic processes for devices of the 20nm node and below at TSMC’s Fab 12 GIGAFAB™. TSMC has also made progress on demonstrating 20nm device processing with EUV lithography using the alpha demo tool located at our IMEC partner site.

- **Mask Technology**
  Mask technology is an integral part of advanced lithography technology. TSMC has developed proprietary resolution-enhancement techniques (RET) that are co-optimized with our in-house mask-making technology. The Company integrates optical proximity correction (OPC) and scanner parameter optimization, and masks them together to provide a total solution in 193nm immersion lithography. TSMC’s mask-making facilities feature state-of-the-art electron-beam mask writers, etchers, inspection, repair, verification, and metrology tools for production at 28nm and R&D at 20nm and beyond. TSMC continues to develop mask technologies for double patterning with 193nm immersion lithography and EUV lithography for applications to the 20nm generation and beyond and participates actively in developing the infrastructure for EUV mask-making. TSMC’s strength in mask technology gives significant and unique benefits to its customers in terms of technical excellence, top quality, fast cycle time, and one-stop service.
Integrated Interconnect and Packaging

The Integrated Interconnect and Package Development Division (IIPD) was formed in late 2008 to develop and deliver an integrated technology solution combining advanced interconnect with packaging technology. The introduction of extreme low-K dielectric (ELK) in 45/40nm adds more challenges among many others to the given tasks. In 2010, the major focus was to resolve interconnect/package related bottlenecks and ensure smooth ramp of 45/40nm first-wave customers’ products. Enhancement in Si backend/bump structure designs, and process optimization in bumping/assembly processes have paved the way for customers’ products delivery with reliable quality. Customers including GPU and FPGA products are in volume production (with die size >20×20mm²).

Advanced Interconnect

In 2010, TSMC continued to lead the foundry segment in demonstrating the lowest resistance/capacitance (RC) -delay interconnect technology in the segment, which is also compatible with advanced package technology.

Copper interconnect resistivity is trending up by generation node because of the size effect. To keep the RC performance for the advanced interconnect, TSMC has developed an extreme low resistance Cu interconnect solution for 28nm and beyond technology nodes. On the 28nm, we also improve effective resistivity of Cu lines to be significantly lower than that projected by the International Technology Roadmap for Semiconductors and demonstrate promising reliability performance.

Advanced Package Development

To achieve “Green package” requirements and to follow the EU code for RoHS, the traditional tin-lead (Sn-Pb) based solder interconnect will be replaced by lead-free (Sn-Ag or Cu post) technology step-by-step. TSMC will continue to develop lead-free package technology (including die sizes, bump pitches, substrate types, etc.) and Fan-in Wafer Level Packaging (Fan-in WLP) for handheld/mobile devices/applications in 2011 to further enhance customers’ product performance and competitiveness.

3D IC

TSMC has committed to work with customers closely to develop cost-effective 3D IC system integration solutions using in-house proprietary through silicon via (TSV) and foundry compatible wafer-level-packaging (WLP) technologies. Our 3D System-in-Package (SiP) solution is a viable alternative for many customers to realize their end product with the best cost and cycle time. TSMC delivers innovations to enable SiP design for the first time. It includes SiP package design, electrical analysis of package extraction, timing, signal integrity, IR drop, and thermal to physical verification of design rule check (DRC) and Layout Verification of Schematic (LVS). Such integrated solution for product realization will be made available to customers in 2012/13.

Advanced Transistor Research

Historically, transistor performance requirement follows different market segments: high performance applications, such as desk top computing; low-operating power applications, such as laptop computers and mobile internet devices; and low standby power applications, such as cell phones for long standby time. TSMC has been the technology leader in the low-operating power applications with G-family transistors and low standby power applications with LP family transistors. As low-operating power applications spread into the high performance domain, TSMC is embracing the challenge to retune our transistor offering to assure customers that they have the most competitive transistor offering from TSMC.

Spectrum of Technology

Beyond the highlights above, TSMC continued to develop a broad mix of new technologies. The Company accelerated its SoC roadmap, including embedded DRAM (eDRAM) and RF with earlier availability, higher integration and more variants.

Embedded DRAM

Continued with TSMC leadership in eDRAM, in 2010 we started to ramp up early production of 40nm LP eDRAM for more efficient memory density and throughput required for bandwidth and graphic applications such as games and DTV. This will be followed by baseband and network applications, using the N40G base logic with 412MHz and 500MHz clock rate. Development also began on N28 eDRAM using HKMG logic as a base technology.

Silicon Germanium BiCMOS Radio Frequency (RF) Technology

SeGi018: Upgraded TSMC SiGe-BiCMOS technology performance to tier-1 SiGe process specifications. For the moment, we are ahead of the ITRS roadmap targets.

Mixed Signal/Radio Frequency (MS/RF) Technology

TSMC delivered a 28nm EM simulation base LC tank design package to facilitate high speed Serdes design. This approach successfully fulfilled requirements for different customized metal schemes in a significantly shorter time. TSMC product enhancement, we developed IPD technology on high R substrate, and provided excellent inductor (Q>50) and precise MiM (C corner<5%) for the RF-FEM (front-end module) segment.

Thin film Resistor: Demonstrated a close to zero TCR TFR which is key for high-precision ADC.

Power IC/BCD Technology

In 2010, TSMC released a multiple-time re-programmable (MTP) non-volatile memory into the existing CO25BCD power management IC technology. A one-time programmable (e-fuse) solution was qualified in 0.25µ/5V and 0.18µ/5V mixed signal technologies and their derivatives (BCD, HV). These features enable customers to trim critical analog characteristics at wafer, package or board level in a cost efficient manner (e-Fuse) or enhance the product functionality (MTP).
Besides continuing various BCD technology developments for DC-DC conversion, TSMC successfully delivered UHV (800V) technology that supports designs for energy-efficient lighting (CFL, LED, E-balaster) and mobile adaptors.

• Panel Driver Technology
In mobile device display drivers, TSMC released two new technologies in 2010: C011HV and N80HV. These technologies are targeted for high resolution displays in smart phones.

To meet more stringent standards in large panel displays (color depth and speed) for new TVs, such as 3D LCD TV, TSMC released two technologies in 2010.

• Microelectromechanical Systems (MEMS) Technology
There are several MEMS technologies for different applications in development at TSMC. In 2010, we worked with a customer to release a gyroscope device in production. We also demonstrated preliminary success in a DNA sequencing device, and made significant progress in our motion sensor platform technology development.

• CMOS Image Sensor Technology
In 2010, TSMC extended our leadership in back-side illumination (BSI) to enable our key customer to win more visible business with popular handheld products. At the same time, BSI wafer processing in 12” bulk-silicon also started risk production with the 65nm 8-megapixel product to be ramped up in early 2011, followed by many others.

TSMC also won the business for another leading CIS provider for 12” technology development, with wafer loading scheduled for 2012.

• Flash/Embedded Flash Technology
In 2010, TSMC delivered a refined low power, extremely low leakage 0.18μm Flash for microprocessor control unit (MCU) applications. The 90nm split gate technology has passed technology qualification. Three macros were qualified. One key customer has delivered Bluetooth engineering samples to their customers. Smart card IP is being qualified with several customers joining shuttle service for product prototyping.

TSMC has engaged with several IDM companies to co-develop embedded flash solutions for automotive, industrial and consumer applications. The technology foundation used includes 90nm, 65nm and 55nm, with the flash cells varying from floating gate and split-gate to hybrid.

5.2.3 Technology Platform
Modern IC designers need sophisticated design infrastructure to achieve acceptable productivity and cycle time. This includes design flow for electronic design automation (EDA), silicon proven building blocks such as libraries and IPs, simulation and verification design kits such as process design kit (PDK) and tech files. All these are built on top of the technology foundation, and each technology needs its own design infrastructure to be usable for designers. This is the concept of a technology platform.

Today’s TSMC technology platforms reflect the culmination of years of work by TSMC and its alliance partners. In 2008, TSMC’s Open Innovation Platform™ was launched to further enhance the Company’s technology platforms, with additional deliverables added on in 2010. The Company unveiled an extension to its IP Alliance program in October to include Soft IP partners.

In April, TSMC announced the foundry segment’s first Analog/Mixed Signal (AMS) Reference Flow, and the second revision of the Radio Frequency Reference Design Kit (RF RDK). The new AMS Reference Flow is TSMC’s first custom design flow that targets leading edge 28nm design challenges, such as Layout Dependent Effects (LDE), Design For Manufacturing (DFM) and Sub-1V, to minimize design barriers and reduce iterations. AMS Reference Flow is a fully integrated multi-vendor program and part of an innovative design package.

The updated RDK provides a solution to common bottlenecks that designers encounter on a daily basis. RDK 2.0 includes step-by-step tutorials and setup scripts to facilitate users going through Circuit Sizing/Design Centering, a comprehensive EM design flow with TSMC PDK, and to analyze substrate noise coupling in RF circuits with TSMC qualified SNA tools.

After the debut of a series of interoperable data formats in iRCX, iDRC, iLVs and iPDK in 2009, TSMC demonstrated its strong commitment to industry users in 2010 with its industry-first iDRC & iLVs runsets in 40nm, and iPDKs in many TSMC advanced process nodes from 0.13μm to 28nm. Working with EDA partners, TSMC publishes quarterly reports for their qualified interoperable tools and versions.

The Soft IP Alliance program aims to improve soft IP readiness for advanced technology nodes and to drive earlier time-to-market. Soft IP has historically been process technology independent and, therefore, not optimized for power, performance and area considerations. Given the ever-increasing need of first-time silicon success and early time-to-market for highly integrated circuits, such as Systems-on-Chip (SoC), close technical collaboration between the foundry and the IP provider is imperative to emphasize this critical trade-off.
iRCX, an interoperable EDA data format, integrates all key process interconnect modeling data, which is increasingly important as chip designs in advanced technologies require detailed views of parasitic effects for the accurate evaluation of chip performance and power consumption. iRCX offers foundry interconnect model data for various applications across the board, covering not only parasitic RC tools at transistor & gate levels, but also the commonly-used tools for Electrical Magnetic (EM) Solver, Field Solver and ElectroMigration (EM)/Current (IR) Drop Analysis. EDA tools that support the iRCX format will be able to receive accurate interconnect modeling data from the iRCX files developed and supported by TSMC.

Executable physical verification runsets for interoperable design rule check (iDRC), interoperable density fill (iFill) and interoperable layout-versus-schematic (iLVs) in TSMC 40nm process technology were delivered to TSMC beta customers in 2010. Design rules for advanced process technologies are more complex and require detailed and accurate descriptions for correct chip layout creation and post-layout analyses. TSMC iDRC and iLVs formats, based on TSMC process requirements, unify process design rules specification and technology file generation, simplify data delivery, and ensure data integrity and interpretation. These are also the deliverables that represent TSMC’s tight collaboration with its EDA partners and mutual customers.

TSMC iPDK unified data model on industry-standard OpenAccess database enables design reuse that is not possible with multiple proprietary PDKs and design databases among various EDA design platforms. It eliminates duplicate PDK development efforts, significantly reduces PDK development, validation and support costs across the design ecosystem, and promotes innovation in analog and full custom design. With a wide range of available iPDKs in TSMC process nodes and industry available EDA design platforms, users are now offered a higher degree of design flexibility in choosing the best tool features to fit their design needs.

To ensure OIP Ecosystem partners’ compliance with TSMC new process requirements, TSMC works with partners to publish the “EDA Tool Qualification Report” on TSMC-Online, providing customers with an actively maintained status of individual EDA tools including DRC, LVs, RC extraction, Placement and Routing. The physical verification tool qualification report of DRC/LVS/iRCX/iFill is updated on quarterly basis, and started to cover iDRC/LVS/iRCX/iFill from 2010. Also new for Year 2010, routing qualification of 28nm was introduced as the design rule becomes Version 1.0.

In order to lower the barrier of technology adoption for customers, TSMC first introduced the Integrated Sign-Off Flow (ISF) in 65nm/55nm in 2009. ISF is a production proven design flow based on TSMC’s internal design expertise accumulated over the years. ISF started to bear fruits in 2010, and enabled a large number of first time 65nm/55nm customers. ISF significantly reduced technology adoption gap in emerging markets such as China.

Entering its 10th year, the TSMC Reference Flow continues to anticipate customer needs in advanced design methodologies, and to serve the purpose of pipe-cleaning EDA tool capabilities. Traditionally the Reference Flow addresses design challenges in power, timing, and design for manufacturing. Reference Flow 11.0 incorporated new requirements associated with leading edge technologies, such as 28nm, and expanded into two new areas: 3D iIC with TSV (through silicon via) and ESL system level design. The former supports heterogeneous integration of multiple dice and to achieve superior timing/power/form factor optimization, while the latter supports the trend of designers moving up to system level, enabling earlier and more accurate tradeoff with accurate TSMC PPA (power, performance and area).

5.2.4 Intellectual Property

A strong portfolio of intellectual property rights strengthens TSMC’s technology leadership and protects our advanced and leading edge technologies. In 2010, TSMC received 434 U.S. patents, 173 Taiwanese patents, 180 PRC patents, and other patents issued in various other countries. TSMC’s patent portfolio now exceeds 13,000 patents worldwide. We continue to implement a unified model for TSMC’s intellectual capital management. Strategic considerations and close alignment with the business objectives drive the timely creation, management and use of our intellectual property.

At TSMC, we have built a process to extract value from our intellectual property by aligning our intellectual property strategy with our R&D, business objectives, marketing, and corporate development strategies. Intellectual property rights protect our freedom to operate, enhance our competitive position, and give us leverage to participate in many profit-generating activities.

We have worked continuously to improve the quality of our intellectual property portfolio and to reduce the costs of maintaining it. We plan to continue investing in our intellectual property portfolio and intellectual property management system to ensure that we protect our technology leadership and receive maximum business value from our intellectual property rights.

5.2.5 Future R&D Plans

Following the significant accomplishments of TSMC’s advanced technologies in 2010, the Company plans to continue to grow its R&D investments. TSMC will further expand its 300mm R&D pilot line to speed up 28nm production ramp and 20nm development. The Company plans to reinforce its exploratory development work on new transistors and technologies, such as 3D structures, strained-layer CMOS, high mobility materials, novel 3D-IC devices with TSV, and interposer. These studies of the fundamental physics of nanometer CMOS transistors are core aspects of our efforts to improve the understanding and guide the design of transistors at advanced nodes. The findings of these studies are being applied to
ensure our continued industry leadership at the 28nm and 20nm nodes. One of TSMC’s goals is to extend Moore’s Law through innovative in-house work, as well as by collaborating with industry leaders and academia to push the envelope in finding cost-effective technologies and manufacturing solutions.

TSMC will continue working closely with international consortia and photolithography equipment suppliers to ensure the timely development of 193nm high-NA scanner technology, EUV lithography, and massively parallel E-Beam direct-write technologies. These technologies are now fundamental to TSMC’s process development efforts at the 20nm and 14nm nodes and beyond.

TSMC continues to work with mask inspection equipment suppliers to develop viable inspection techniques, a collaborative partnership to help ensure the Company maintains its leadership position in mask quality and cycle time and continue to meet aggressive R&D, prototyping and production requirements.

With a highly competent and dedicated R&D team, and unwavering commitment to innovation, TSMC is confident of its ability to deliver the best and most cost-effective SoC technologies for customers, and to support the Company’s business growth and profitability.

TSMC R&D future major project summary:

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<th>Project Name</th>
<th>Description</th>
<th>Risk Production (Estimated Target Schedule)</th>
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<td>28nm technology for both digital and analog products</td>
<td>2010 - 2011</td>
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<tr>
<td>20nm logic platform technology and applications</td>
<td>Next-generation technology for both digital and analog products</td>
<td>2012</td>
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<tr>
<td>14nm logic platform technology and applications</td>
<td>Exploratory technology for both digital and analog products</td>
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<td>3D-IC</td>
<td>Cost-effective solution with better form factor and performance for SIP</td>
<td>2012 - 2013</td>
</tr>
<tr>
<td>Next-generation lithography</td>
<td>EUV and multiple E-Beam to extend Moore’s Law</td>
<td>2011 - 2012</td>
</tr>
<tr>
<td>Long-term research</td>
<td>Special SoC technology (including new NVM, MEMS, RF, analog) and 14nm transistors</td>
<td>2012 - 2014</td>
</tr>
</tbody>
</table>

The above plans account for roughly 70% of the total corporate R&D budget in 2011, which is currently estimated to be around 7-8% of 2011 revenue.

5.3 Manufacturing Excellence

5.3.1 GIGAFAB™ Fabrifications

TSMC’s 12-inch fabs are a key part of its manufacturing strategy. TSMC currently operates two 12-inch GIGAFAB™ fabrication facilities – Fab 12 and Fab 14 – whose combined capacity reached 2,520,000 12-inch wafers in 2010. Production within these two facilities supports 0.13μm, 90nm, 65nm, 40nm, and 28nm process technologies, and their sub-nodes. Part of the capacity is reserved for research and development work and currently supports 20nm, 14nm and beyond technology development. A third GIGAFAB™ fabrication, Fab 15, located in Taichung’s Central Taiwan Science Park, is on track for equipment move-in during the second quarter of 2011.

TSMC has developed a centralized fab manufacturing management for the customers’ benefit of same quality and reliability performance, greater flexibility of demand fluctuations, faster yield learning and time-to-volume, and minimized costly product re-qualification.

5.3.2 Engineering Performance Optimization

Highly sophisticated information technology (IT) solutions, such as advanced equipment control and fault detection, are implemented to optimize TSMC equipment performance and improve production efficiency.

Advanced analytical methods identify critical equipment and process parameters that are linked to device performance. Methodologies such as virtual metrology and yield management integrate Advanced Process Control (APC), Fault Detection Classification (FDC), Statistical Process Control (SPC), and Circuit Probe data in order to optimize equipment performance to match device performance. Accurate modeling and control at each process stage drives intelligent module loop control.

The process control hierarchy dispatched via sophisticated computer-integrated manufacturing system enable optimization from equipment to end product, which achieves precision and lean operation in a high product-mix semiconductor manufacturing environment.
5.3.3 Precision and Lean Operations

TSMC’s unique manufacturing infrastructure is tailored for a high product mix foundry environment. Following its commitment to manufacturing excellence, TSMC has equipped a sophisticated scheduling and dispatching system, implemented industry-leading automated materials handling systems, and employed Lean Manufacturing approaches to provide customers with on-time-delivery and best-in-class cycle time. Real-time equipment productivity monitoring, analysis, diagnosis and control minimize production interruption and maximize cost effectiveness.

5.3.4 450mm Wafer Manufacturing Transition

The Company contributes to infrastructure development of 450mm wafer transition, which will enable industry continue path of cost reduction. TSMC will continue to work with International SEMATECH, ISMI, material and equipment suppliers on the next wafer size transition, lithography strategy, efficient tool design, new material development and eco-friendly process development.

Recently, we made plans to set up 450mm pilot line in 2013 to 2014, and production line in 2015 to 2016.

5.3.5 Raw Materials and Supply Chain Risk Management

In 2010, TSMC continued running monthly Supply Chain Risk Management meetings to integrate Company resources from materials management, fab operations, risk management and quality management in lowering supply chain risk. TSMC worked with its suppliers to enhance the performance of quality, delivery, risk management, and to support Green procurement, environmental protection and safety.

Raw Materials Supply

<table>
<thead>
<tr>
<th>Major Materials</th>
<th>Major Suppliers</th>
<th>Market Status</th>
<th>Procurement Strategy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw Wafers</td>
<td>F.S.T MEMC</td>
<td>These five suppliers together provide over 85% of the world’s wafer supply. Each supplier has multiple manufacturing sites in order to meet customer demand, including plants in North America, Asia, and Europe.</td>
<td>▪ TSMC’s suppliers of silicon wafers are required to pass stringent quality certification procedures. ▪ TSMC procures wafers from multiple sources to ensure adequate supplies for volume manufacturing and to appropriately manage supply risk. ▪ TSMC maintains competitive price and service agreements with its wafer suppliers, and, when necessary, enters into strategic and collaborative agreements with key suppliers. ▪ TSMC regularly reviews the quality, delivery, cost and service performance of its wafer suppliers. The results of these reviews are incorporated into TSMC’s subsequent purchasing decisions. ▪ A periodic audit of each wafer supplier’s quality assurance systems ensures that TSMC can maintain the highest quality in its own products.</td>
</tr>
<tr>
<td>Chemicals</td>
<td>Air Products</td>
<td>These six companies are the major suppliers for bulk and specialty chemicals.</td>
<td>▪ Most suppliers have relocated many of their operations closer to TSMC’s major manufacturing facilities, thereby significantly improving procurement logistics. ▪ The suppliers’ products are regularly reviewed to ensure that TSMC’s specifications are met and product quality is satisfactory.</td>
</tr>
<tr>
<td>Litho Materials</td>
<td>A2 Nissan</td>
<td>These five companies are the major suppliers for worldwide litho materials.</td>
<td>▪ TSMC works closely with its suppliers to develop materials able to meet application and cost requirements. ▪ TSMC and suppliers periodically conduct improvement programs of their quality, delivery, sustainability and green policy, to ensure continuous progress of TSMC’s supply chain.</td>
</tr>
<tr>
<td>Gases</td>
<td>Air Liquide</td>
<td>These four companies are the major suppliers of specialty gases. The products of these four suppliers are interchangeable.</td>
<td>▪ The majority of the four suppliers are located in different geographic locations, minimizing supply risk to TSMC. ▪ TSMC conducts periodic audits of the suppliers’ quality assurance systems to ensure that they meet TSMC’s standards.</td>
</tr>
<tr>
<td>Slurry, Pad, Disk</td>
<td>Cabot Microelectronics</td>
<td>These seven companies are the major suppliers for CMP materials.</td>
<td>▪ Most suppliers have relocated many of their operations closer to TSMC’s major manufacturing facilities, thereby improving procurement logistics and mitigating supply chain risk. ▪ TSMC conducts periodic audits of the suppliers’ quality assurance systems to ensure that they meet TSMC’s standards.</td>
</tr>
</tbody>
</table>
5.3.6 Quality and Reliability

TSMC is committed to providing customers with the best quality wafers for their products. Our Quality and Reliability (Q&R) services aim to achieve “quality on demand” to fulfill customers’ needs regarding time-to-market, reliable quality, and market competition over a broad range of products.

In the technology development and customer product design stage, Q&R technical services assist customers to design-in their product reliability requirements. Since 2008, Q&R has worked with R&D to successfully establish and implement new qualification methodology for high-k/metal gate (HKMG). Q&R also works with design services on embedded memory, high voltage, e-Fuse and MEMS IP developments to expand TSMC’s design portfolio. In 2010, Q&R worked with R&D and the design service team to develop an integrated R&D and design quality platform that included items such as SPICE, DRM, DFM, IP/lib. In package reliability, Q&R extends characterization to the system level by establishing Power Cycling capability and methodology.

Q&R has deployed systems to ensure robust quality in managing production and in design services including third-party IP management as the Company meets the business requirements of customers. In 2010, Q&R implemented innovative statistical matching methodologies for manufacturing quality enhancement, including matching of facility, metrology and process tools, wafer acceptance test (WAT) data and reliability performance.

To sustain production quality and minimize risk to customers when deviations occur, manufacturing quality monitoring and event management span all critical stages – from raw material supply, mask making, and real-time in-process monitoring, to bumping, wafer sort and reliability performance. Advanced failure and materials analysis techniques are also developed and effectively deployed in process development, customer new product development, and product manufacturing. In 2010, analytical techniques traditionally used in a laboratory environment were adapted to aid in the release and monitoring of advanced Fab tools and processes for the 40nm and 28nm technology nodes.

In compliance with the electronic industry’s lead-free and green IC package policy, Q&R qualified and released lead-free bumping to satisfy customer demands and made lead free bump package possible for 0.13μm, 45nm and 40nm technology products by collaborating with the major outsource assembly & testing subcontractors (OSAT) in 2010. This has enabled TSMC customers to introduce and ramp lead-free products with excellent assembly quality. Q&R will continue to enhance this collaboration platform for 28nm and future technologies to support customers from wafer processing to assembly and testing quality management. For mainstream technologies, Q&R has been building reliability testing and monitoring to ensure excellent manufacturing quality of automotive, high-voltage products, CMOS image sensors and MEMS products.

In addition to the silicon wafer business, TSMC has expanded into new areas related to solid state lighting and solar businesses, for which Q&R is engaged in establishing new, rigorous standards of quality and reliability leveraging our years of experience in the semiconductor industry.

TSMC Q&R is also responsible for leading the Company towards the ultimate goal of zero-defect production, through the use of continuous improvement programs. Periodic customer feedback indicates that products shipped from TSMC have consistently met or exceeded their field quality and reliability requirements. In 2010, the effectiveness of the TSMC quality management system was verified by a third-party audit to comply with ISO/TS 16949:2009 and IECQ QC080000 certificates requirements.
5.4 Customer Partnership

5.4.1 Customers

TSMC’s global customers have diverse product specialties and excellent performance records in various segments of the semiconductor industry. Fabless customers include: Altera Corporation, Advanced Micro Devices, Inc., Broadcom Corporation, Marvell Semiconductor Inc., NVIDIA Corporation, Qualcomm Inc. and MediaTek Inc. IDM customers include: Analog Devices Inc., Freescale Semiconductor Inc., NXP Semiconductors, and Texas Instruments Inc.

Customer Service

TSMC believes that providing superior customer service is critical to enhancing customer satisfaction and loyalty, which is the path to retaining existing customers, attracting new customers, and strengthening customer partnerships. TSMC strives to provide world-class, high-quality, efficient and professional integrated services to achieve optimum service experience for our customers and, in return, to gain customer’s trust and sustain Company profitability.

To facilitate customer interaction and information access on a real-time basis, TSMC has offered a suite of web-based applications that provide a more active role in design, engineering, and logistics, collectively branded as EFOUNDRY® service. The design collaboration focuses on content availability and accessibility, with attention to accurate and updated information at each level of the design lifecycle. The engineering collaboration includes online access to pilot lots, wafer yields, wafer acceptance test (WAT) analysis, and quality reliability data. Logistics collaboration provides access to data updated three times a day on the status of a given wafer lot during fabrication, assembly and testing, final testing, order and shipping.

Customer Satisfaction

TSMC conducts an annual customer satisfaction survey (ACSS) to assess customer satisfaction and to ensure that their needs and wants are adequately understood and addressed. In the survey, all active customers are invited to participate either by web or interview survey through an independent consultancy. Continual improvement plans based upon customer feedback are an integral part of this business process. TSMC has maintained a focus on customer survey data as a key indicator of corporate performance – not just of past performance, but also as a leading indicator of future performance. TSMC has acted on the belief that satisfaction leads to loyalty, and customer loyalty leads to higher levels of retention and expansion.

Customers Accounted for at Least 10% of Annual Consolidated Net Sales

<table>
<thead>
<tr>
<th></th>
<th>2010 Net Sales (NT$ thousands)</th>
<th>2010 As % of 2010 Total Net Sales</th>
<th>Relation to TSMC</th>
<th>2009 Net Sales (NT$ thousands)</th>
<th>2009 As % of 2009 Total Net Sales</th>
<th>Relation to TSMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Customer A</td>
<td>38,619,756</td>
<td>9%</td>
<td>None</td>
<td>Customer A</td>
<td>30,276,650</td>
<td>10%</td>
</tr>
<tr>
<td>Customer B</td>
<td>37,202,785</td>
<td>9%</td>
<td>None</td>
<td>Customer B</td>
<td>30,162,597</td>
<td>10%</td>
</tr>
<tr>
<td>Others</td>
<td>343,715,370</td>
<td>82%</td>
<td>Others</td>
<td>235,302,992</td>
<td>80%</td>
<td></td>
</tr>
<tr>
<td>2010 Total Net Sales</td>
<td>419,537,911</td>
<td>100%</td>
<td></td>
<td>2009 Total Net Sales</td>
<td>295,742,239</td>
<td>100%</td>
</tr>
</tbody>
</table>
5.4.2 Design Enablement

In order to lower the design barriers for customers to design on TSMC technologies, the Company offers extensive design support to its customers through a direct design support team as well as via alliance partners. TSMC’s technology platform provides a solid foundation for design enablement.

Tech File and PDK

Customers heavily leverage tech files and process design kits (PDK) provided by TSMC, as evidenced by more than 20,000 downloads in 2010. TSMC also experiences high demand on PDK for mainstream technologies and is increasing resources to support that demand.

Library and IP

TSMC and its alliance partners offer TSMC’s customers a rich portfolio of libraries and IPs. These reusable building blocks are essential for many design projects. In 2010, over half of new tape-outs to TSMC adopted one or more libraries or IPs from TSMC and/or its IP partners. To support the high demand, TSMC also invested resources to expand the library and IP portfolio. The total number of library or IP in the portfolio increased to 3,005 in 2010 from about 2,221 in 2009.

Design Methodology and Flow

TSMC released the first foundry-specific Integrated Sign-Off Flow in April 2009. Initially targeting 65nm process node with planned extensions into other process technology nodes, the Integrated Sign-Off Flow supports advanced design techniques for low power and design-for-manufacturability. With validated libraries and IP, qualified EDA tools, a full set of proper technology files, and automated installation scripts, Integrated Sign-Off Flow significantly shortens the time it normally takes a design team to set up the design environment and flow before starting the design project. The built-in advanced design methodology and proven sign-off scripts further shortens the design cycle, and improves tape-out quality.

Two New Programs

In another first for the foundry segment, TSMC announced in April 2010 the first Analog/Mixed Signal (AMS) Reference Flow, and the second revision of the Radio Frequency Reference Design Kit (RF RDK).

TSMC’s AMS Reference Flow is our first custom design flow that targets a host of design challenges associated with leading edge 28nm – Layout Dependent Effects (LDE), Design for Manufacturing (DFM) and Sub-1V – to minimize design barriers and reduce iterations. AMS Reference Flow is a fully integrated multi-vendor program and part of an innovative design package.

The Company expanded its IP Alliance program in 2010 to incorporate soft IP. The goal is to improve soft IP readiness for advanced technology nodes and to drive earlier time-to-market. Due to its history of independence from process technology, soft IP was not optimized for power, performance and area considerations. With the increasing need of first-time silicon success and early time-to-market for highly integrated circuits, such as Systems-on-Chip (SoC), close technical collaboration between the foundry and IP provider is imperative.

5.5 Employees

5.5.1 Human Capital

Human capital is one of the most important assets of TSMC. TSMC strives to provide employees with a challenging, enjoyable and rewarding work environment. In 2010, TSMC was named the “Most Admired Company in Taiwan” by Commonwealth Magazine for the 14th consecutive year.

At the end of 2010, TSMC had more than 33,000 employees worldwide, including 3,142 managers and 12,729 professionals. Female managers comprised 11.2% of all managers, and non-Taiwanese nationals comprised 9.6% of all TSMC managers and professionals. The following tables summarize TSMC’s workforce structure at the end of February, 2011:

**TSMC Workforce Structure**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Manager</td>
<td>2,792</td>
<td>3,142</td>
<td>3,189</td>
</tr>
<tr>
<td>Professional</td>
<td>9,861</td>
<td>12,729</td>
<td>12,904</td>
</tr>
<tr>
<td>Assistant Engineer/Clerical</td>
<td>761</td>
<td>2,650</td>
<td>2,672</td>
</tr>
<tr>
<td>Technician</td>
<td>11,052</td>
<td>14,711</td>
<td>14,904</td>
</tr>
<tr>
<td>Gender</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Male (%)</td>
<td>50.7%</td>
<td>53.4%</td>
<td>53.5%</td>
</tr>
<tr>
<td>Female (%)</td>
<td>49.3%</td>
<td>46.6%</td>
<td>46.5%</td>
</tr>
<tr>
<td>Education</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ph.D.</td>
<td>3.5%</td>
<td>3.3%</td>
<td>3.3%</td>
</tr>
<tr>
<td>Master’s</td>
<td>32.8%</td>
<td>31.7%</td>
<td>31.9%</td>
</tr>
<tr>
<td>Bachelor’s</td>
<td>20.7%</td>
<td>25.9%</td>
<td>25.9%</td>
</tr>
<tr>
<td>Other Higher Education</td>
<td>16.5%</td>
<td>14.3%</td>
<td>14.1%</td>
</tr>
<tr>
<td>High school</td>
<td>26.5%</td>
<td>24.8%</td>
<td>24.8%</td>
</tr>
<tr>
<td>Average Age (years)</td>
<td>37.8</td>
<td>32.3</td>
<td>32.4</td>
</tr>
<tr>
<td>Average Years of Service (years)</td>
<td>6.0</td>
<td>5.5</td>
<td>5.5</td>
</tr>
<tr>
<td>Total</td>
<td>24,466</td>
<td>33,232</td>
<td>33,669</td>
</tr>
</tbody>
</table>
5.5.2 Recruitment

Attracting new employees, and retaining and motivating existing employees are key to the success of TSMC’s human resources strategy. TSMC believes in equal opportunity employment. Recruitment is conducted via an open selection process and is based on the candidate’s ability to fulfill the needs of each position, regardless of race, gender, age, religion, nationality, or political affiliation. In order to seek out the best talents around the world, TSMC employs a number of recruiting programs, including academic/corporate collaboration programs, Joint Development Program in Campus, summer internships, job fairs, and Technology Talents Career Symposium. During 2010, TSMC recruited 185 managers, 4,012 professionals, 1,919 assistant engineer/clerical and 4,599 technicians.

The past successes of TSMC have relied on contributions from all employees, and our future development will need a keen sense of commitment to continue to succeed in competition to come. Therefore, in 2010, we recruited around 2,100 qualified existing outsourced staff to be regular workforce. We deeply believe that employees are our greatest asset, and doing so will not only allow us to take care of more colleagues, it will also bolster morale and inspire us to do our best together.

5.5.3 People Development

A key to TSMC’s long-term success has been our employee development strategy, which emphasizes continuous learning especially important for success in this challenging economic environment. A tailor-made individual development plan is established for each employee appropriate to the employee’s development needs. Employees are provided with a comprehensive network of resources, including on-the-job training, coaching, mentoring, job rotation, on-site courses, e-learning, and external learning opportunities.

TSMC provides employees with a wide range of on-site general, professional and management training programs. In addition to external experts engaged as trainers, hundreds of TSMC employees are trained as qualified instructors for training courses. During 2010, TSMC conducted 1,465 internal training sessions, the total training hours achieved 968,457 and a total of 569,941 attendees participated in those trainings; employees on average attended 29.14 hours of training. The total training expenses were NT$70 million. TSMC’s training programs include:

- Management Training: includes development training programs tailored to the needs of managers at all levels. These include New Manager Program, Experienced Manager Program, and Senior Manager Program, as well as other elective courses.
- General Training: refers to training required by government regulations and Company policies. Such training includes industry-specific safety, workplace health and safety, quality, fab emergency response team, languages, and personal effectiveness training.
- Professional/Functional Training: provides technical and professional training required by various functions within the Company, offering training courses on equipment engineering, process engineering, accounting, and information technology, among others.
- Direct Labor (DL) Training: DL training enables production line employees to acquire the knowledge, skills and attitudes they need to perform their job well. It also helps employees to pass required tests in order to be certified for operating equipment. Training includes DL Skill Training, Technician “Train-the-Trainer” Training, and Manufacturing Leader Training.
- New Employee Training: includes new employee basic training and job orientation.

TSMC has established the Procedure of Employee Training and Education, which not only enables the on-site training courses but also best suits Company and individual development objectives through external training courses. Under the guideline, employees are encouraged to participate in various training programs, and subsidies are provided when taking short-term courses, credit courses and degrees.

5.5.4 Employee Satisfaction

To enhance employee satisfaction, TSMC continuously promotes programs devoted to employee benefits, employee care, employee rewards, and employee communication. TSMC works hard to enrich its employees’ working experience by providing an environment that is challenging yet enjoyable.

Employee Benefits Programs

- TSMC’s Employee Welfare Committee plans and implements various welfare programs, including hobby clubs, art and cultural seminars, employee outings, TSMC Sports Day, and TSMC Family Day. In addition, TSMC provides holiday bonuses, marriage bonuses, condolence allowances and emergency subsidies.
- To ensure that employees have all the comforts and conveniences they need while at work, TSMC provides on-site cafeterias, dry-cleaning, travel, banking, haircut services, housing, and commuting assistances.
- Health improvement programs and psychological consultation services are available to employees to ensure their physical and psychological well-being.
- In order to promote a healthy lifestyle, TSMC Sports Center offers a variety of workout facilities and is open to all employees and their family members. In addition, daycare centers are available at Hsinchu and Tainan sites to meet employees’ need for childcare.

Employee Recognition

In order to recognize employees’ outstanding achievement, TSMC runs various award programs including the Outstanding Engineer Award for each fab and the Total Quality Excellence Conference Award. During 2010, TSMC employees were recognized nationally, including the National Model Worker Award, the Top 10 National Outstanding Managers Award, the Outstanding Engineer Award, and the Outstanding Young Engineer Award.
Employee Communication
TSMC values two-way communication and is committed to keeping the communication channels between the management level and their subordinates, as well as between the peers, open and transparent. Our unceasing efforts lie in the reinforcement of mutual and timely employee communication, based on existing platforms, which in turn fosters harmonious labor relations and creates a win-win situation for the company and the employees.

Regular communication meetings are held for the various levels of managers and employees. Periodic employee satisfaction surveys are conducted. eSilicon Garden, an electronic internal publication, is issued on a bi-weekly basis with topics ranging from work to fun. These all help maintain the unobstructed flow of information between TSMC and its employees.

In order to ensure that employees’ opinions and voices are heard, and their issues are addressed and solved, impartial and smooth voice submission mechanisms are in place to provide timely support:

- Complaints regarding major management, financial and auditing issues are directed to the following channels, which handle the complaints with high level of confidentiality: 1) The Independent Audit Committee and 2) The Ombudsman system led by a selected Vice President.
- The Suggestion Box for employees to express their opinions regarding their work and the work environment in general.
- HR Call Center and employee care teams in each fab take care of the issues related to employees’ work and personal life. The Company also sets and promotes policies and measures for ensuring gender equality in accordance with employment laws and sexual harassment prevention policies to create a fair work environment for employees of both genders.

5.5.5 Retention
From the employee’s initial adaptation to professional and career development, TSMC works hard to retain outstanding employees through creating an innovative, challenging, and fun environment. We are committed to:

- Setting up retention and counseling plans for different groups. For example, TSMC employs a “Buddy System” to help new employees fit in quickly through the assistance provided by senior employees.
- Enabling employees to enhance professional knowledge and to pursue further career development through numerous employee development programs.
- Establishing a synergized welfare platform and providing an environment for employees’ work-life balance; enhancing employees’ loyalty and commitment through employee engagement programs.

5.5.6 Compensation
TSMC’s compensation program includes a monthly salary, an employees’ cash bonus based on quarterly business results, and an employee profit sharing when the Company distributes its profit each year.

To raise TSMC’s competitiveness in recruiting, TSMC made a structural salary increase in 2010, and started the distribution of the employees’ cash bonus quarterly based on the Company’s financial performance to share the rewards of employees’ hard work in a timely fashion.

The purpose of the employee cash bonus and profit sharing program is to reward employees’ contributions appropriately, to encourage employees to work consistently to ensure the success of TSMC, and to link employees’ interests with those of TSMC’s shareholders. The Company determines the amount of the cash bonus and profit sharing based on operating results and industry practice in the Republic of China. The amount and form of the employee cash bonus and profit sharing are determined by the Board of Directors based on the Compensation Committee’s recommendation and the employee profit sharing is subject to shareholders’ approval at the Annual Shareholders’ Meeting. Individual awards are based on each employee’s job responsibility, contribution and performance.

In addition to providing employees of TSMC’s overseas subsidiaries with a locally competitive base salary, the Company grants short-term and long-term bonuses as a part of total compensation. The performance bonus is a short-term incentive and is granted in line with local regulations, market practices, and the overall operating performance of each subsidiary. The long-term incentive bonus is awarded based on TSMC’s financial performance and is vested over the course of several years in order to encourage long-term employee commitment and development within the Company.

5.5.7 Retirement Policy
TSMC’s retirement policy is in accordance with the provisions in the Labor Standards Law and Labor Pension Act of the Republic of China.
5.5.8 Ethics and Business Conduct

Ethics Values
Integrity is the most important core value of TSMC’s culture. TSMC is committed to act ethically in all aspects of our business; constantly and vigilantly promoting integrity, honesty, fairness, accuracy, and transparency in all that we say and do.

TSMC’s Code of Ethics and Business Conduct (“Code”) requires that each of TSMC’s employees bears a heavy personal responsibility to preserve and to protect TSMC’s ethical values and reputation. In so doing, each of us: must not advance our personal interests at the expense of, or in conflict with the Company; must refrain from corruption, unfair competition, fraud, waste and abuse; must not undertake any practices detrimental to TSMC, the environment and to society; must abide by both the spirit and letter of all applicable laws, rules and regulations; and must avoid any efforts improperly to influence the decisions of anyone, including government officials, agencies, and courts, as well as our customers, suppliers, and vendors.

In order to continue to build an environment of innovation, technology leadership, and sustainable profitable growth, this Code requires that we must promote business relationships founded upon an unwavering respect for the intellectual property rights, proprietary information and trade secrets of TSMC, our customers, and others; and the proper use of the Company’s assets, not for personal use, but for achieving TSMC’s vision for many years to come.

All employees, officers and Board members must whole-heartedly embrace and practice this Code. TSMC’s management must set the best example of integrity and ethical conduct. TSMC’s officers, especially our CEO, CFO, and General Counsel, with oversight from our Board, are responsible for the full, fair, accurate, timely, and understandable financial accounting and financial disclosure in reports/documents filed by the Company with securities authorities and in all TSMC public communications/disclosures.

Code Administration and Disciplinary Action
All employees, officers and managers must comply with this Code and its related procedures. TSMC expects our customers, suppliers, vendors, advisors and others with which we come into contact to understand and respect the Company’s ethics and culture.

When an employee finds or suspects a breach of this Code, he/she should report it immediately to any of the following persons: their supervisor; the Function Head of Human Resources; the Company’s Ombudsmen; or to the Chairman of the Company’s Audit Committee, depending on the nature of the suspected breach.

The Company will discipline employees who violate this Code in accordance with the Company’s “Employee Recognition and Discipline Policy” (including the possibility of the termination of employment).

5.6 Material Contracts

Shareholders Agreement
Term of Agreement:
Effective as of 03/30/1999 and may be terminated as provided in the agreement
Contracting Parties:
Koninklijke Philips Electronics N.V. (Philips) and EDB Investments Pte Ltd. (EDBI)
(In September 2006, Philips assigned its rights and obligations under this agreement to Philips Semiconductors International B.V. which has now been renamed NXP B.V. In November 2006, NXP B.V. and TSMC purchased all SSMC shares owned by EDBI; EDBI is no longer a contracting party to this agreement.)
Summary:
TSMC, Philips and EDBI had formed a Singapore joint venture “Systems on Silicon Manufacturing Company Pte Ltd.” (SSMC) for providing IC foundry services. Philips Semiconductor (now NXP B.V.) and TSMC are committed to purchasing a certain percentage of SSMC’s capacity.

Technology Cooperation Agreement
Term of Agreement:
03/30/1999 - 03/29/2004, automatically renewable for successive five-year terms until and unless either party gives written notice to terminate one year before the end of then existing term
Contracting Party:
Systems on Silicon Manufacturing Company Pte Ltd. (SSMC)
Summary:
TSMC agreed to transfer certain process technologies to SSMC, and SSMC agreed to pay TSMC a certain percentage of the net selling price of SSMC products.

Patent License Agreement
Term of Agreement:
12/20/2007 - 12/31/2017
Contracting Party:
A multinational company
Summary:
The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting company.

Manufacturing, License, and Technology Transfer Agreement
Term of Agreement:
04/01/2004 - 03/31/2006, automatically renewable for successive one-year terms until and unless both parties decide otherwise by mutual consent in writing
Contracting Party:
Vanguard International Semiconductor Corporation (VIS)
Summary:
VIS reserves certain capacity to manufacture TSMC products on mutually agreed terms. TSMC may also transfer certain technologies to VIS, for which it will in return receive royalties from VIS.
Patent License Agreement  
Term of Agreement:  
11/01/2002 - 10/31/2012  
Contracting Party:  
A multinational company  
Summary:  
The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting party.

Patent License Agreement  
Term of Agreement:  
01/01/2001 - 12/31/2011  
Contracting Party:  
A multinational company  
Summary:  
The parties entered into a cross licensing arrangement for certain semiconductor patents. TSMC pays license fees to the contracting party.

Amended Research and Development Collaboration Agreement  
Term of Agreement:  
01/01/2009 - 12/31/2009, renewable on annual basis upon mutual agreement  
Contracting Party:  
NXP B.V.  
Summary:  
The parties entered into research and development collaboration to develop advanced semiconductor technologies.

Purchase Agreement  
Effective Date of Agreement:  
12/30/2010  
Contracting Party:  
Powerchip Technology Corporation  
Summary:  
TSMC spent NT$2.9 billion to acquire from Powerchip Technology Corporation the substructure of the building under construction located in Hsinchu Science Park.

Note: TSMC is not currently party to any other material contract, other than contracts entered into in the ordinary course of our business. The Company’s “Significant Commitments and Contingencies” are disclosed in the “Financial Information” of Annual Report (II), page 69-70.