TSMC Delivers Interoperable EDA Formats for Advanced Process Technologies

Multiple Interoperable Technology Files Now Available for 65nm, 40nm and 28nm Chip Designs

Hsinchu, Taiwan, R.O.C. – April 7, 2010 - Taiwan Semiconductor Manufacturing Company, Ltd. (TWSE: 2330, NYSE: TSM) has made available several unified and interoperable electronic design automation (EDA) technology files for its 65 nanometer (nm), 40nm and 28nm process nodes. The design technology file suite includes interoperable process design kit (iPDK), interoperable design rule check (iDRC), layout-versus-schematic (iLVS), and interoperable interconnect extraction (iRCX).

The iPDK, iDRC, iLVS, and iRCX technologies are developed and jointly validated with TSMC’s EDA partners under the industry-wide Interoperability Project that is an integral part of the company’s Open Innovation Platform™ (OIP).

Process and design rules for advanced semiconductor manufacturing technologies are more complex and require detailed, accurate descriptions for correct chip layout creation, simulation and post-layout verification and analysis.  TSMC collaborates with major EDA ecosystem partners who are part of the OIP Interoperability Project to define and develop a unified architecture and interoperable formats based on TSMC process requirements.  The company’s EDA partners support the new format in their tools and qualify tool accuracy against actual silicon measurements. This qualification process eliminates data inconsistency, reduces tool evaluation time and improves design accuracy.

TSMC developed its first 40nm iDRC/iLVS in collaboration with development partners Mentor and Synopsys as well as QA/validation partners Magma and Cadence. TSMC also developed its first 65nm iPDK in collaboration with Synopsys and Ciranova as development partners in addition to QA/validation partners Magma and Springsoft. Both interoperable technology files have been under customer evaluation since July of last year. After extensive testing, the 65nm iPDK, the 40nm iPDK, and the 65nm and 40nm iDRC and iLVS technology files are now available for production designs.

TSMC is now adding the 40nm and 28nm iRCX files to its robust portfolio of 65nm iRCX technology files that have been used in production designs since early 2009.

“TSMC collaborates with multiple EDA vendors to create and validate interoperable EDA
formats that accelerate data delivery and ensure the integrity and accuracy of advanced process technology data,” said ST Juang, senior director of Design Infrastructure Marketing at TSMC. “The latest version of the iPDK, iDRC, iLVS, and iRCX technology files are production design ready and incorporating the valuable feedback we received from customers and ecosystem partners during the beta test period. The new unified EDA data format provides designers the ability to select qualified EDA tools that match their design needs, improve compliance with TSMC processes, and ensure design accuracy for first-time silicon success.”

Availability
The TSMC 65nm iPDK is available now. The 40nm iPDK, 65nm and 40nm iDRC and iLVS, and 28nm iRCX files are expected to be available in the second quarter of 2010. Technology files and the interoperable EDA format tool qualification results can be accessed at the TSMC Online customer design portal http://online.tsmc.com/online/ or by contacting TSMC account management and support executives for details.

About TSMC Open Innovation Platform™
The TSMC Open Innovation Platform promotes timely innovation amongst the semiconductor design community, design ecosystem partners and TSMC’s IP, design implementation, process technology and backend services. The Open Innovation Platform includes a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that efficiently empowers innovation throughout the supply chain and enables the creation and sharing of newly-created revenue and profitability. TSMC’s AAA initiative is a critical part of the Open Innovation Platform, providing the accuracy and quality required by ecosystem interfaces and collaborative components.

About TSMC
TSMC is the world’s largest dedicated semiconductor foundry, providing the industry’s leading process technology and the foundry’s largest portfolio of process-proven libraries, IPs, design tools and reference flows. The Company’s managed capacity in 2009 totaled 9.96 million (8-inch equivalent) wafers, including capacity from two advanced 12-inch GIGAFABs™, four eight-inch fabs, one six-inch fab, as well as TSMC’s wholly owned subsidiaries, WaferTech and TSMC China, and its joint venture fab, SSMC. TSMC is the first foundry to provide 40nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

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