TSMC Unveils Reference Flow 8.0 to Address 45nm Design Challenges

Lowers entry barriers to design for TSMC 45nm and other advanced process technologies

Hsinchu, Taiwan - June 4, 2007 - Taiwan Semiconductor Manufacturing Company, Ltd. (TSE: 2330, NYSE: TSM) today unveiled Reference Flow 8.0, the latest generation of the foundry’s design methodology that increases yields, lowers risks and improves design margins.

Reference Flow 8.0 supports TSMC’s 45nm process technology with advanced standard cell, standard I/O, and SRAM compiler. Key features address new design challenges at 45nm, including statistical timing analysis for intra-die variation, automated DFM hot-spot fixing, and new dynamic low-power design methodologies.

Reference Flow 8.0 supports TSMC’s Active Accuracy Assurance initiative, which defines standards of accuracy for all partners in TSMC’s design ecosystem, as well as for TSMC itself. Reference Flow 8.0 focuses on ease of use, providing a reference of qualified design building blocks that give designers a proven path from specification to tape out.

Reference Flow 8.0 not only supports TSMC’s advanced process technologies such as 45nm, 65nm, and 90nm, but also provides mature, proven design flows for mainstream technologies from 0.13-micron to 0.25-micron.

“TSMC’s 45nm process technology requires ever-deeper collaborations with EDA vendors and other partners in our design ecosystem,” said Kuo Wu, deputy director of design service marketing at TSMC. “Reference Flow 8.0 provides a seamless link between the designers and advanced process technologies, and is supported by TSMC’s unrivalled real-world manufacturing technology and capacity.”

Enhanced Statistical Timing Analysis

Reference Flow 7.0 introduced the first foundry design methodology to include inter-die statistical timing analysis to accurately determine the timing effects of manufacturing process variations. Reference Flow 8.0 expands on this capability by offering intra-die statistical timing analysis along with statistical leakage and statistical timing optimization. Statistical leakage provides a more precise analysis of leakage that reflects actual manufacturing outcomes. Statistical timing optimization helps reducing the need for over-design and enables more effective timing closure. These features enable designers to optimize design margins and increase yields.
Design for Manufacturability (DFM)

Reference Flow 8.0 provides further improvements in DFM methodology, which allows designers to address potential manufacturing challenges during the design process, rather than post-processing after tape-out. Among the new features are automated DFM hot spot fixing to eliminate the need for manual correction and DFM electrical variability consideration, which monitors parametric performance shifts caused by DFM effects. Increased automation, integrated analysis, and optimization capabilities shorten design cycles by enabling designers to anticipate DFM issues and quickly take necessary measures.

Low Power Design

Reference Flow 8.0 includes a number of new and innovative power reduction techniques including TSMC’s new AVS (Adaptive Voltage Scaling) which enables reduction of active power consumption for next-generation mobile devices. A dual power rail SRAM design enables more dynamic power reduction, long channel device innovations cut power consumption due to leakage. Coarse-grain power gating and other techniques employed in standard cells further reduce overall standby leakage. The Common Power Format (CPF) enables significant improvement in automated low-power design methodology. Together these features extend battery life for portable devices and reduce packaging and cooling costs.

About TSMC

TSMC is the world’s largest dedicated semiconductor foundry, providing the industry’s leading process technology and the foundry industry’s largest portfolio of process-proven libraries, IP, design tools and reference flows. The Company’s total managed capacity in 2006 exceeded seven million (8-inch equivalent) wafers, including capacity from two advanced 12-inch GigaFabs, four eight-inch fabs, one six-inch fab, as well as TSMC’s wholly owned subsidiaries, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. TSMC is the first foundry to provide 65nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

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