TSMC Unveils Two New Reference Flows

Reference Flow 11.0 hosts systems level design methodology; AMS Reference Flow 1.0
Addresses Key Advanced Technology Design Challenges

Hsinchu, Taiwan, R.O.C. – June 8, 2010 - Taiwan Semiconductor Manufacturing Company, Ltd. (TWSE: 2330, NYSE: TSM) today introduced Reference Flow 11.0 and Analog/Mixed Signal (AMS) Reference Flow 1.0. Both are key collaborative components of TSMC’s recently-announced extension of its Open Innovation Platform™.

Reference Flow 11.0, focuses on Electronic System Level (ESL) design, SoC Interconnect Fabric, and two dimensional and three dimensional integrated circuits (2-D/3-D ICs) using through silicon via (TSV) technology. AMS Reference Flow 1.0 offers advanced multi-vendor AMS design flow fully integrated with an innovative TSMC AMS design package to manage the growing complexity of process effects as well as design complexity at 40nm and 28nm process nodes.

Reference Flow 11.0 Electronic System Level Design and SoC Interconnect Fabric
TSMC’s Reference Flow 11.0 is the first generation to host electronic system level (ESL) design. TSMC plays the key role to elevate the indices of power, performance and area (PPA) into an ESL design flow. This enables designers to explore meaningful PPA among different system architectures. Specifically, the ESL flow includes virtual platform prototyping, high level synthesis (HLS) and ESL to RTL verification. In addition, SoC Interconnect Fabric flow is introduced to address SoC timing issue due to long interconnect. It brings the new capability to resolve the issues early at the architecture level while optimizing system performance and latency.

System in Package (SiP) and 2-D/3-D IC
System in Package (SiP) and 2-D/3-D IC technologies enable designers to integrate heterogeneous technologies, realize end product design and strengthen competitive advantages in terms of cost, performance and time-to-market. Reference Flow 11.0 builds on top of the SiP solution first introduced in Reference Flow 10.0 last year by adding support of custom designed die in SiP structure, broadband package extraction, and mechanical analyses. Through-silicon-via (TSV) encourages short and high-density interconnection to replace IO pad cells in the connection between chips. As a result, customers receive the benefit of reduced power while achieving superior system performance because of the higher signal bandwidth. Reference Flow 11.0 addresses new 3-D IC with through-silicon-via (TSV) design and analysis capabilities, including automatic placement and routing (APR), physical
verification, and thermal analysis for two-die stack.

28nm Power, Performance and DFM Design Enablement
Reference Flow 11.0’s new low power features include extended Common Power Format (CPF) and Unified Power Format (UPF) support in IP modeling for low power features and power constraint verification. Multiple advanced stage-based On-Chip Variation (OCV) optimization and analysis tables in clock and data paths, instead of a single AOCV table, drive improved performance and provide a more realistic look at timing to remove redundant design margins.

A new variation-aware custom design flow, a new electrical DFM feature, reduces gap between pre-layout simulation and post layout simulation by evaluating layout effect prior to layout completion. Reference Flow 11.0 includes new DFM fixing capabilities early in the design cycle. These capabilities include interoperable LPC hotspot format to enable LPC hotspot fixing in multiple EDA LPC and layout tools, and LPC pattern matching to speed up LPC hotspot identification and fixing in automatic placement and routing (APR) tools, and dummy VIA insertion in router, thus shorten the iteration time to fix DRC and timing violations.

Foundry’s First Analog/Mixed Signal Design Flow
The TSMC AMS Design Flow 1.0’s design package includes industry-first layout-dependent effect (LDE) aware design methodology and TSMC-specific LDE engine, complete DFM-aware analog layout guideline and checker utility, advanced analog base cell (ABC) design, and a comprehensive design configuration management environment, all integrated seamlessly on top of 28nm interoperable process design kit (iPDK) and OpenAccess database.

The advanced AMS design flow includes a robust front-end design and simulation platform for the analysis of design sensitivity, yield, multi process corners, noise effect, IR drop and electromigration(EM) issues. The AMS physical flow includes constraint-driven analog placement and routing technology for fast layout prototyping, semi-automatic rule-driven layout assistance, and a demonstration of a PLL system design budgeting and loop filter layout synthesis capability. Physical verification flow includes accurate 3D field solver based extraction with intelligent RC reduction, and full DRC/LVS sign-off and dummy pattern insertion and extraction.

The TSMC AMS Reference Flow 1.0 is developed and fully validated in collaboration with multiple EDA partners including Apache Design Solutions, Berkeley Design Automation, Cadence, Ciranova, EdXact, Magma Design Automation, Mentor, Pyxis Technology, Silicon Frontline, Solido Design Automation, and Synopsys.
About the Open Innovation Platform™
The TSMC Open Innovation Platform™ promotes timeliness-driven innovation among the semiconductor design community, ecosystem partners, and TSMC’s complete technology portfolio. The Open Innovation Platform includes a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that efficiently empowers innovation throughout the supply chain thereby enabling creation and sharing of newly created revenue and profitability. TSMC’s Active Accuracy Assurance (AAA) initiative is a critical part of the Open Innovation Platform, providing the accuracy and quality required by ecosystem interfaces and collaborative components.

About TSMC
TSMC is the world’s largest dedicated semiconductor foundry, providing the industry’s leading process technology and the foundry’s largest portfolio of process-proven libraries, IPs, design tools and reference flows. The Company’s managed capacity in 2009 totaled 9.96 million (8-inch equivalent) wafers, including capacity from two advanced 12-inch GIGAFABs™, four eight-inch fabs, one six-inch fab, as well as TSMC’s wholly owned subsidiaries, WaferTech and TSMC China, and its joint venture fab, SSMC. TSMC is the first foundry to provide 40nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please visit http://www.tsmc.com.

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TSMC Spokesperson
Ms. Lora Ho
Vice President and CFO
Tel: 886-3-566-4602