TSMC Extends Design Methodology Leadership to 28nm with Reference Flow 10.0

Introduces SiP design solutions for the first time and continues to drive differentiated features in power, performance and DFM

Hsinchu, Taiwan – July 22, 2009 – Taiwan Semiconductor Manufacturing Company, Ltd. (TWSE:2330, NYSE: TSM) today unveiled Reference Flow 10.0, the latest version of its industry-leading design methodology to lower design obstacles, improve design margins, and increase yields. Reference Flow 10.0 is one of the key collaborative components of the Open Innovation Platform™. The newest generation of the company’s reference flow continues the tradition of driving advances in design methodology, addresses new design challenges of 28nm process technology and delivers innovations to enable System-in-Package (SiP) design.

28nm Design Enablement
TSMC’s Open Innovation Platform (OIP) paves the way for EDA tools to be ready for 28nm. OIP enables design and process technology co-optimization in the early stage of R&D, and ensures required EDA tool enhancements to happen correctly and timely. Specifically for Reference Flow 10.0, TSMC went beyond physical verification of DRC, LVS and extraction which heavily depend upon 28nm process requirements, and engaged early with EDA partners to qualify their place and route tools for TSMC 28nm.

System in Package (SiP)
System-on-Chip (SoC) has been the focus in the previous nine generations of the TSMC Reference Flow starting in 2001. Reference Flow 10.0 introduces SiP design solutions for the first time including SiP package design, electrical analysis of package extraction, timing, signal integrity, IR drop, and thermal to physical verification of DRC and LVS. These SiP technologies enable customers to explore their implementation and integration strategies, realize end product design and strengthen competitive advantages in terms of cost, performance, and time-to-market.

Expanded EDA Collaboration
New to the flow is a RTL-to-GDSII chip implementation track from Mentor Graphics, in support of customers’ EDA usage. Reference Flow 10.0 further enables existing ecosystem partners Altos, Anova, Apache, Azuro, Cadence, CLK DA, Extreme DA, Magma, Nannor, and Synopsys to bring EDA innovations to customers through collaboration with TSMC.
**Differentiated Features in Power, Performance and DFM**

New low power features in Reference Flow 10.0 include support for pulsed latch, a new low-power implementation scheme for power saving, and hierarchical low power automation, multi-corner power/timing co-optimization, multi-corner low power Clock Tree Synthesis (CTS), vectorless power analysis and more, enabling more effective power-aware implementation and power analysis. To drive greater performance, advanced stage-based On-Chip Variation (OCV) optimization and analysis is made available for the first time, enabling customers to get a more realistic look at timing for the purpose of removing redundant design margins. A new electrical DFM feature is introduced for customers to take into consideration the timing impact of “silicon stress effect,” thus helping to increase yields.

**About the Open Innovation Platform™**

The TSMC Open Innovation Platform™ promotes timeliness-driven innovation among the semiconductor design community, ecosystem partners, and TSMC’s complete portfolio. The Open Innovation Platform includes a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that efficiently empowers innovation throughout the supply chain thereby enabling creation and sharing of newly created revenue and profitability. TSMC’s Active Accuracy Assurance (AAA) initiative is a critical part of the Open Innovation Platform, providing the accuracy and quality required by ecosystem interfaces and collaborative components.

**About TSMC**

TSMC is the world’s largest dedicated semiconductor foundry, providing the industry’s leading process technology and the foundry’s largest portfolio of process-proven libraries, IP, design tools and reference flows. The Company’s total managed capacity in 2008 exceeded 9 million 8-inch equivalent wafers, including capacity from two advanced 12-inch GigaFabs™, four eight-inch fabs, one six-inch fab, as well as TSMC’s wholly-owned subsidiaries, WaferTech and TSMC (China), and its joint venture fab, SSMC. TSMC is the first foundry to provide 40nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC, please visit [http://www.tsmc.com](http://www.tsmc.com).